MODEL NAME : BAP10(15")/BAP20(17")
PROJECT CODE : ANRBAP1000/ANRBAP2000
PCB NO :
DAC00004000 LA-D751P M/B(NV)
DAC00005000 LA-D751P M/B(NV_G3)
DA4002AV000 LS-D751P LOGO_15/B
DA80017I000 LS-D752P LOGO_17/B
DA4002B000S LS-D753P PWR_15/B
DA4002AW000 LS-D754P PWR_17/B
DA80017J000 LS-D755P IO_12L/B
DA4002AY000 LS-D757P TRON_LCD_15/B
DA4002AZ000 LS-D758P TRON_REAR_15/B
DA80017K000 LS-D759P IO_14L/B
DA4002D4000 LS-D75AP TRON_LCD_17/B
DA4002D5000 LS-D75BP TRON_REAR_17/B
DA4002D7000 LS-D75CP TRON_FRONT_15/B
DA4002D8000 LS-D75DP TRON_FRONT_17/B
DA30000W300 LF-D751P Head_15/B
DA30000W400 LF-D752P Head_17/B
DA30000W401 LF-D752P Head_17/B(For LOGO_15/B)
DA30000SY00 LF-D753P TRON_15/B
DA30000WX00 LF-D754P TRON_17/B

ZZZ PCB@

PCB 1JM LA-D751P REV0 M/B NV 16

DAC00004000

ZZZ PCBR1@

PCB 1JM LA-D751P REV1 M/B NV 16

DAC00004010

ZZZ PCBR3@

PCB 1JM LA-D751P REV1 MB NV TRIP 16 A31!

DAC00004011

ZZZ DAZR1@

PCB BAP10 LA-D751P LS-D751P-2P/D754P/D757P-DP 02

DAZ1JM00100

ZZZ DAZR3@

PCB BAP10 LA-D751P LS-D751P-2P/D754P/D757P-DP 02 TRI A31 !

DAZ1JM00101

HDMI@ ROYALTY HDMI W/LOGO

Part Number	Description
RO0000003HM	HDMI W/Logo:RO0000003HM

Layout Dell logo

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REV: X00
PWB: XXXXX
DATE: 1450-06

BAP10/BAP20 Skylake/Kabylake-H 45W

Skylake/Kabylake PCH with nVidia N17P/N17E

REV : 1.0 (A00)

2016.08.15

@ : Nopop Component

EMI@,ESD@,RF@ : EMI/ESD/RF part

CONN@ : Connector Component

@EMI@,@ESD@,@RF@ : Total debug Component

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Title: Cover Page

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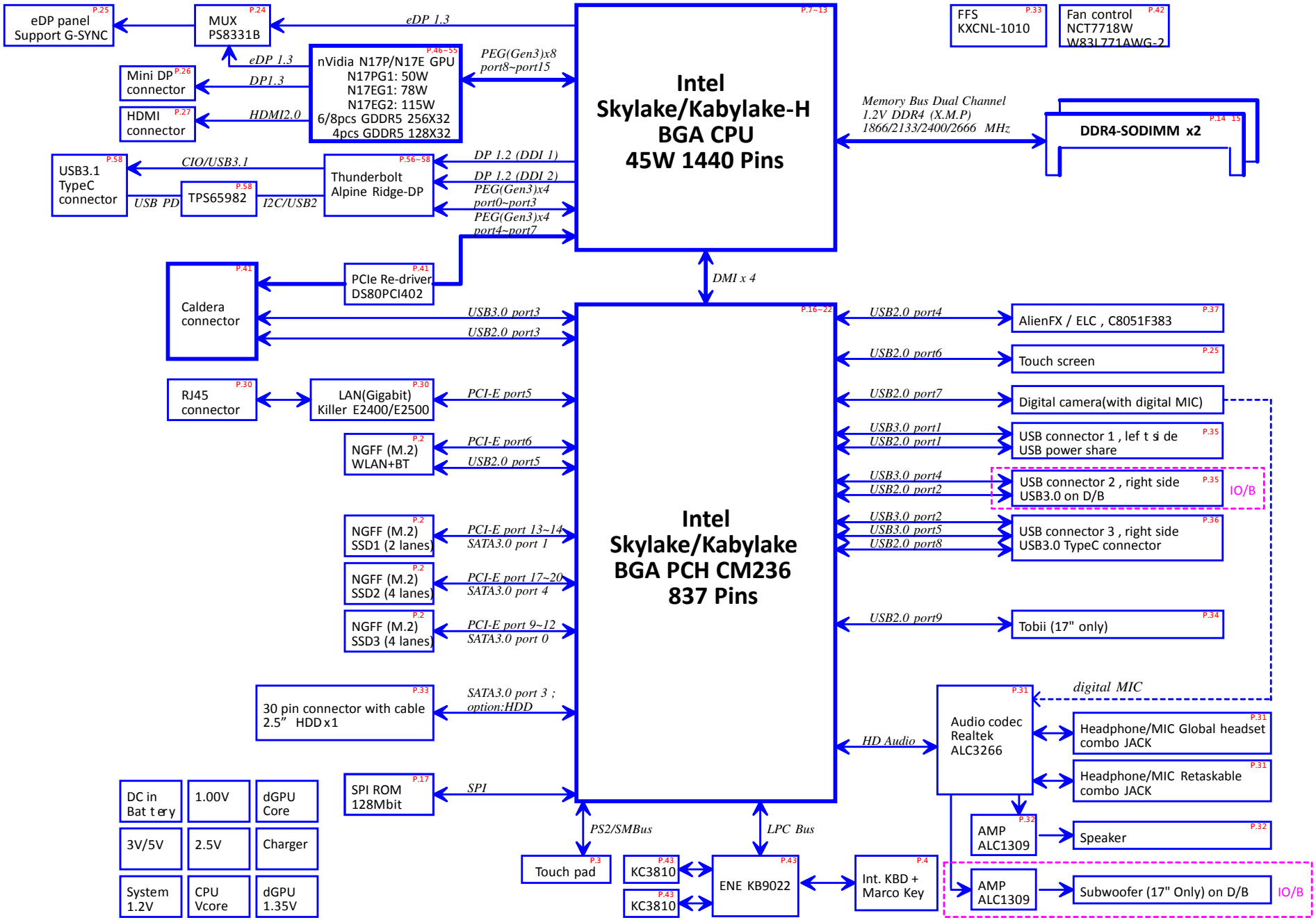
Block Diagram



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Title: **Block Diagram**

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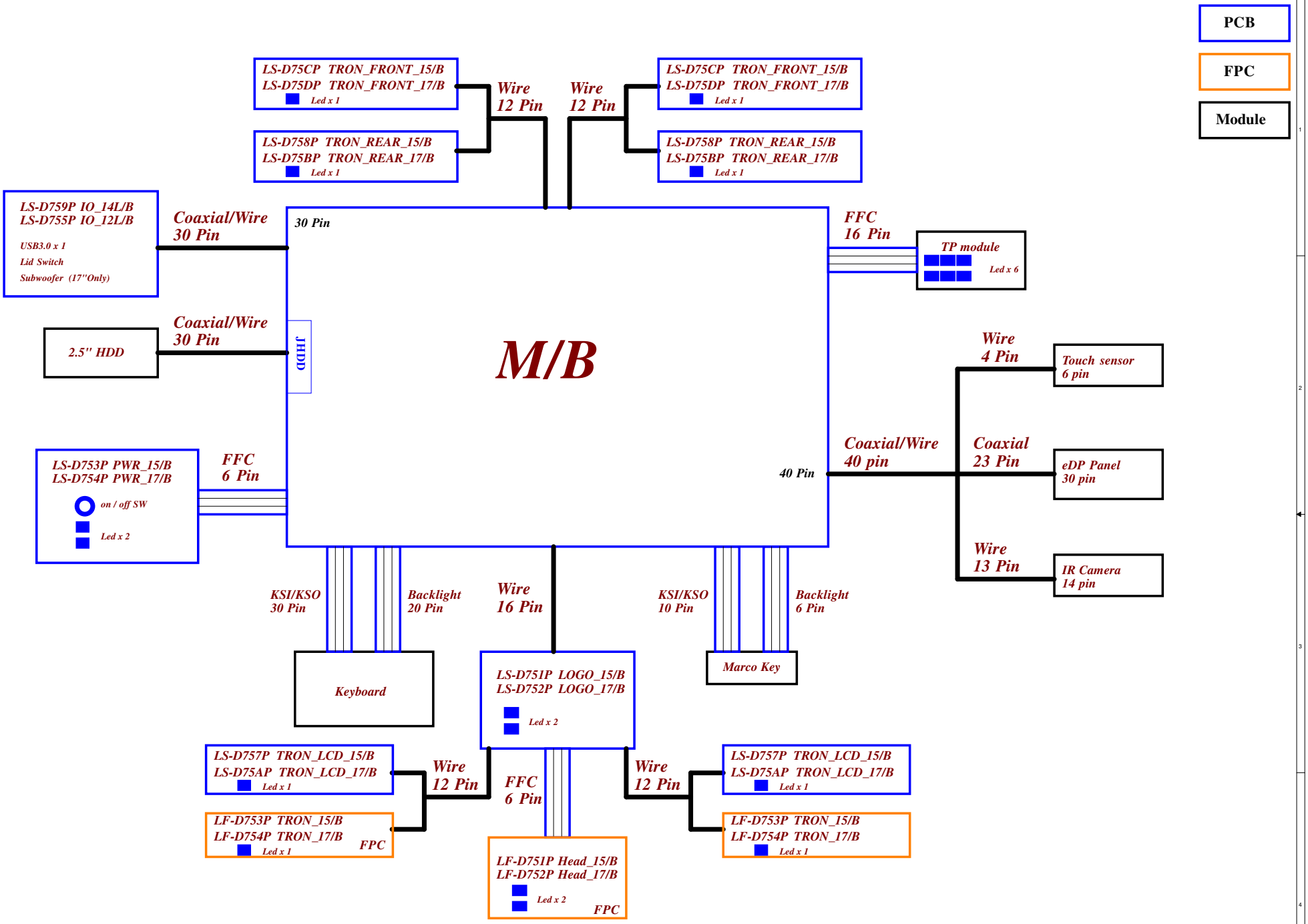
Date: Tuesday, August 16, 2016 Sheet 2 of 82



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Title: Cable Routing Diagram

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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x13	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A	NVIDIA Graphic
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF	AMD Graphic
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0	
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF	

Voltage Rails

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VS	+1.8VS power rail for GPU	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Board ID TABLE

SKL ID		PCB Revision
NV		
0		EVT
1		DVT-1
2		DVT-1.1
3		DVT-2 / DVT-2.1
4		GC6
5		Pilot build

KBL ID		PCB Revision
NV		
1		EVT
6		DVT-1 / DVT-1.1
7		GC6
8		DVT-2
9		Pilot build

PCH-H CM236

HSIO	USB3	PCIe	SATA3	Function
1	1			JUSB1,type A
2	2			JUSBC2,type C
3	3			Caldera
4	4			JIO,IO/B
5	5			JUSBC2,type C
6	6			
7	7	1		
8	8	2		
9	9	3		
10	10	4		
11		5		LAN
12		6		WLAN
13		7		
14		8		
15		9	0	JSSD3 M.2 2280 SATA PCIe x4
16		10	1	
17		11		
18		12		
* 22		16	3	JSSD5/HDD SATA
21		15		
20		14	1	JSSD1 SATA/PCIe x2
19		13	0	
23		17	4	JSSD2 M.2 2280 SATA PCIe x4
24		18	5	
25		19		
26		20		

USB2	Function
1	JUSB1(Powershare)
2	JIO(IO/B)
3	Caldera
4	ELC
5	Bluetooth
6	Touch screen
7	Camera
8	JUSBC2
9	Tobii
10	
11	
12	
13	
14	

* PCIe 13~16 in "Lane Reversal Mode". (HSIO Port 19~22)

Symbol Note :

Digital Ground

Analog Ground

CPU,C
DDR,D
GPU,DP,HDMI,EDP,V
LAN,L
AUDIO,A
NGFF,N
USB,U
CALDERA,M
HDD,S
ELC,E
FAN,F
TP,T
KBC,K
DC,O

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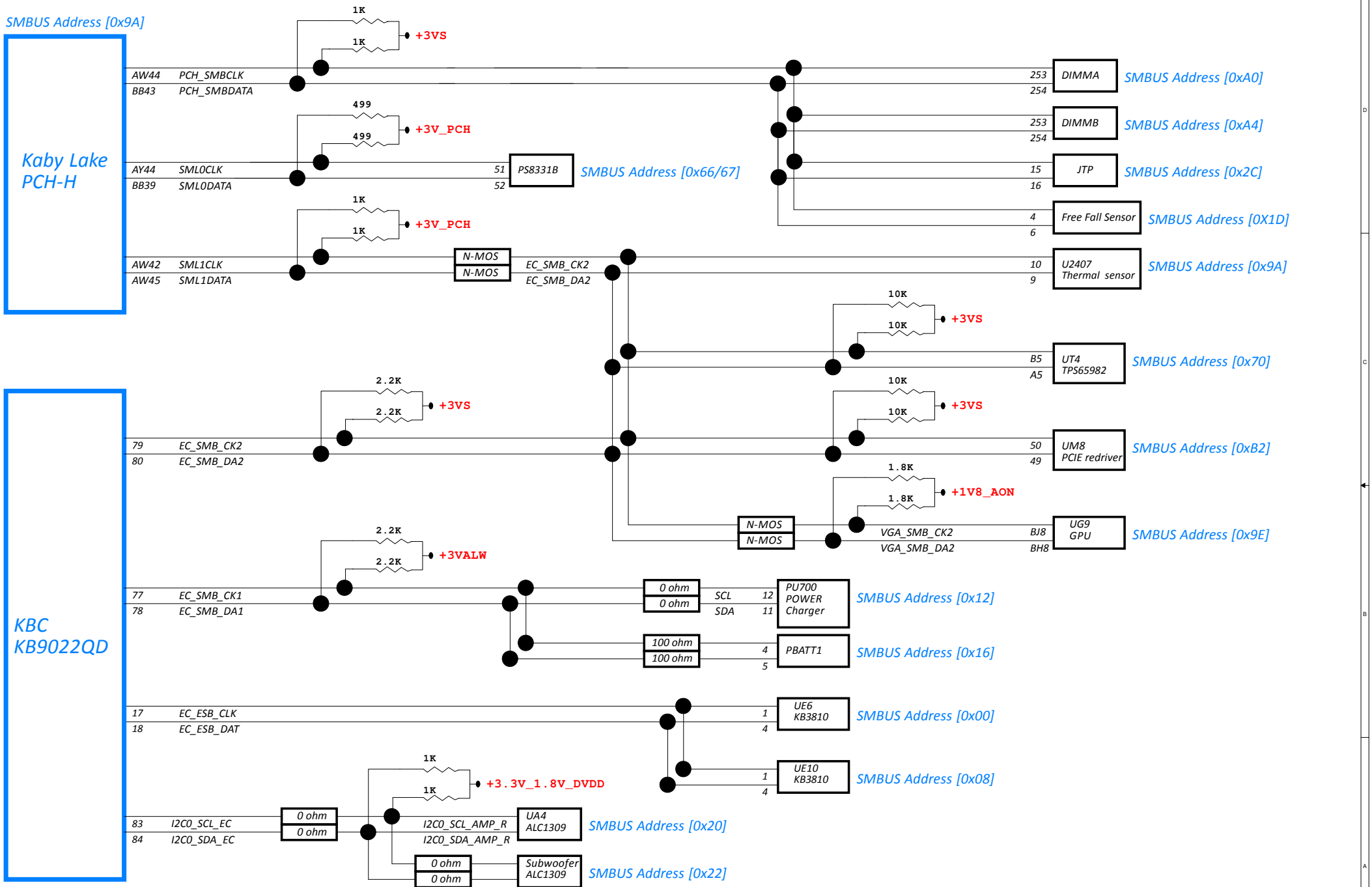

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Title: **SMBus Block Diagram**

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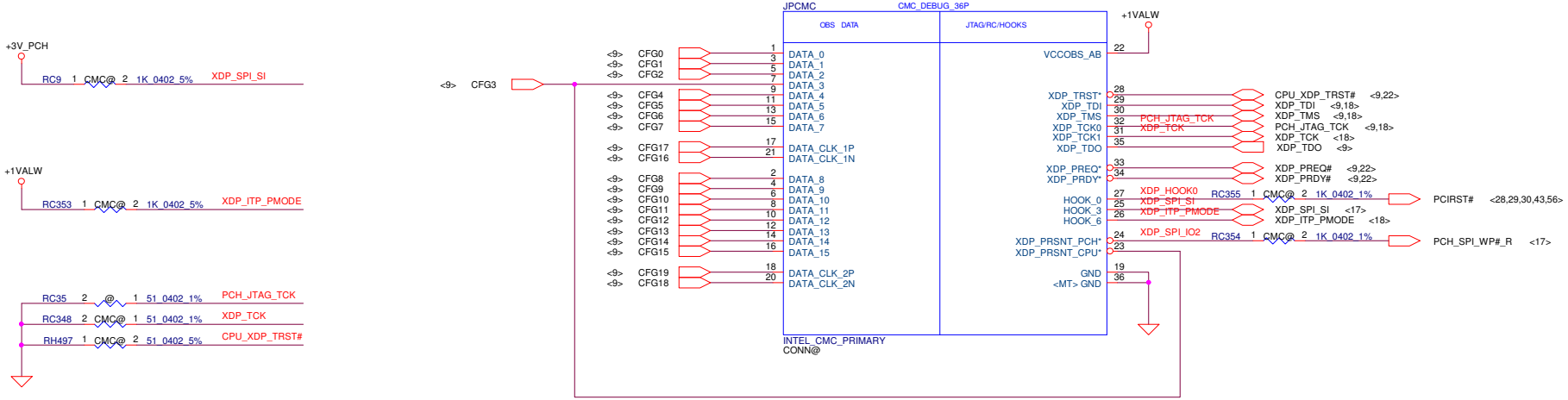

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Title: **CMC Conn**

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Skylake-H CPU
i7K : i7-6820HK
i7H : i7-6700HQ
i5H : i5-6300HQ

CPU1
S IC CL8066202194730 SR2FL R0 2.7G BGA
SA000097D1L
Si7KR1@

CPU1
S IC CL8066202194635 SR2FQ R0 2.6G FCBGA
SA000095Z1L
Si7HR1@

CPU1
S IC CL8066202194632 SR2FP R0 2.3G FCBGA
SA000096Q1L
Si5HR1@

CPU1
S IC CL8066202194730 SR2FL R0 2.7G A31!
SA000097D2L
Si7KR3@

CPU1
S IC CL8066202194635 SR2FQ R0 2.6G A31!
SA000095Z2L
Si7HR3@

CPU1
S IC CL8066202194632 SR2FP R0 2.3G A31!
SA000096Q2L
Si5HR3@

Kabylake-H CPU
i7K :
i7H :
i5H :

CPU1
S IC A31 CL8067702869810 QL2X A0 2.7G FCBGA 1440
SA0000A130L
Ki7KES@

CPU1
S IC A31 CL8067702869811 QL3X A0 2.4G BGA 1440
SA0000A150L
Ki75ES@

Thunderbolt RX <Reverse>

Caldera RX <Reverse>

GPU RX <Reverse>

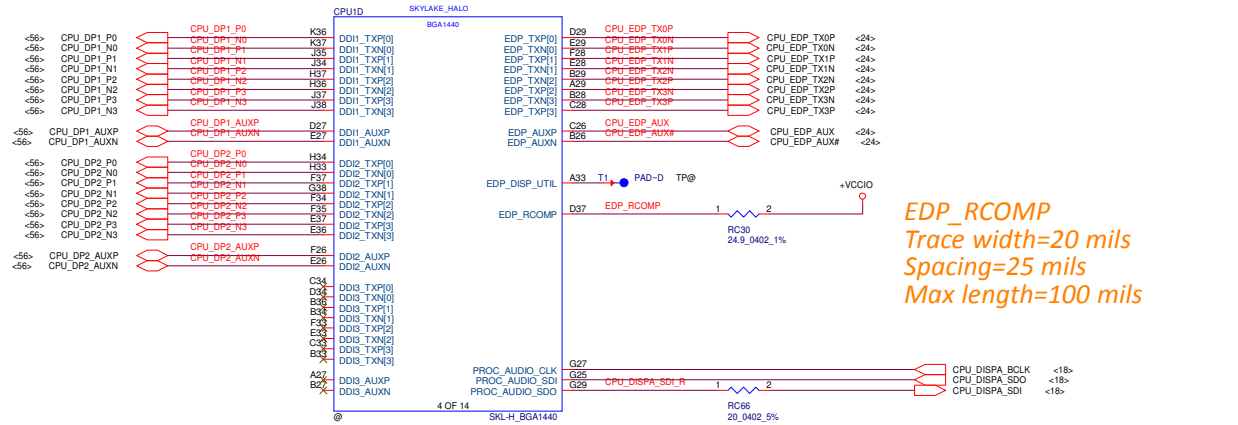
Thunderbolt TX <Reverse>

Caldera TX <Reverse>

GPU TX <Reverse>

PEG_RCOMP
Trace width=12 mils
Spacing=15 mils
Max length= 400 mils

EDP_RCOMP
Trace width=20 mils
Spacing=25 mils
Max length=100 mils



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Compal Electronics, Inc.

Title: CPU(1/7) DMI,PEG,DDI,EDP

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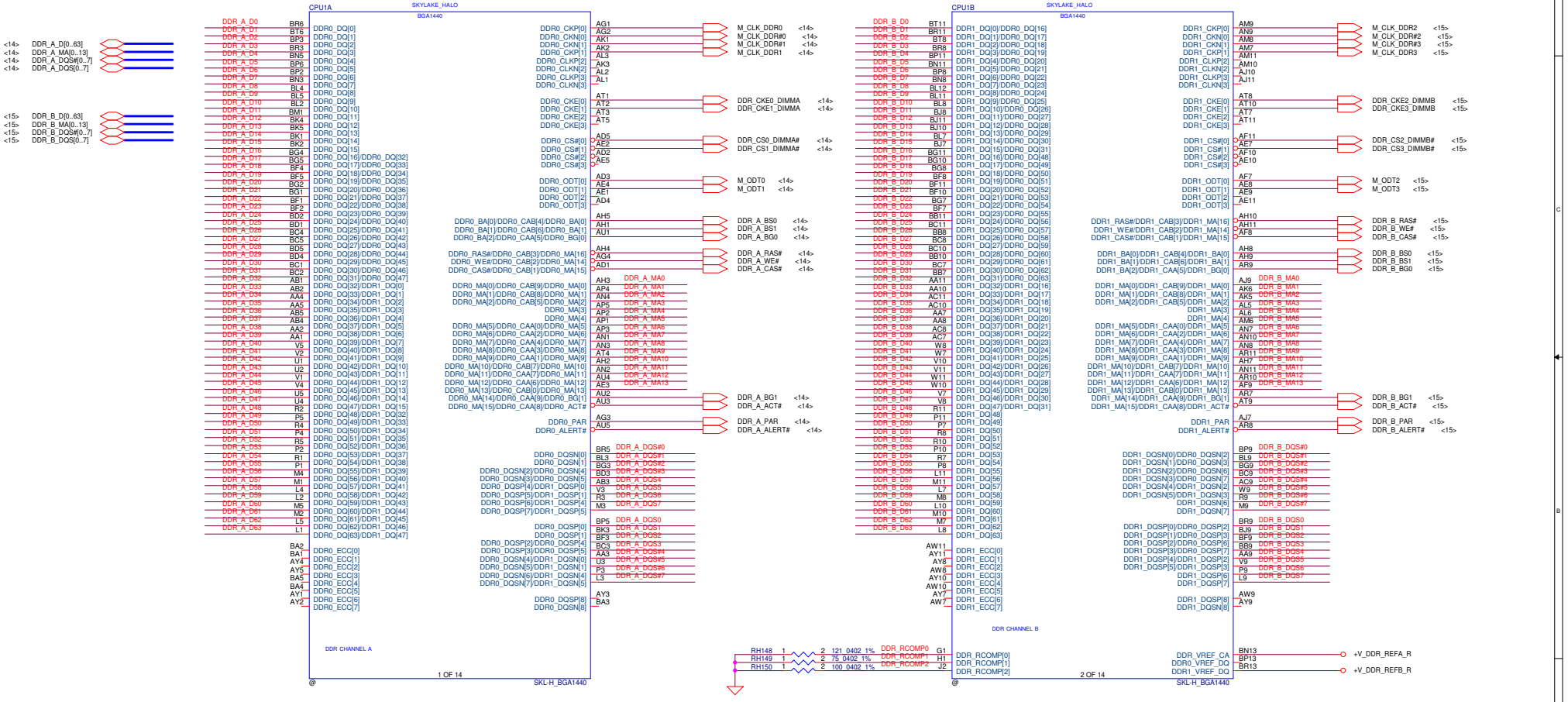
Interleave



DDR_RCOMP0 :
DDR_RCOMP1 :
DDR_RCOMP2 :
Trace width=12~15 mils
Spacing=20 mils
Max length= 500 mils

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Title: **CPU(2/7) DDR4**

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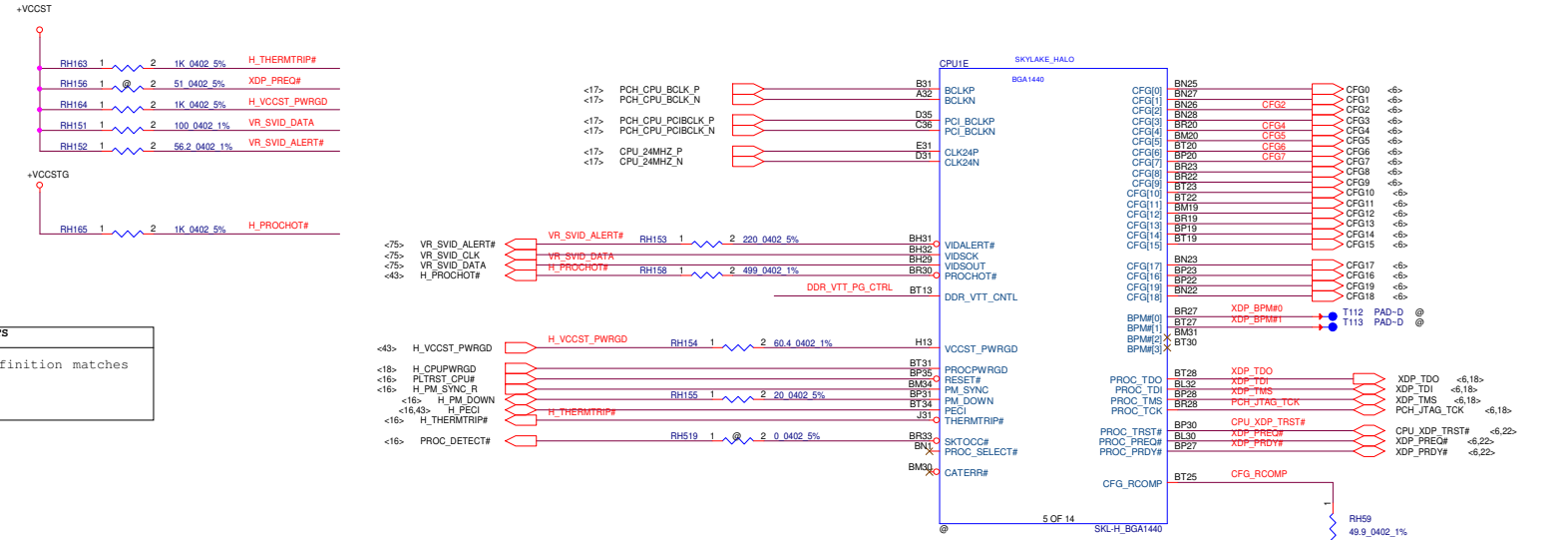
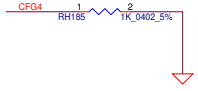
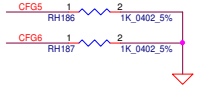


PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

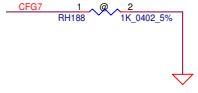
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

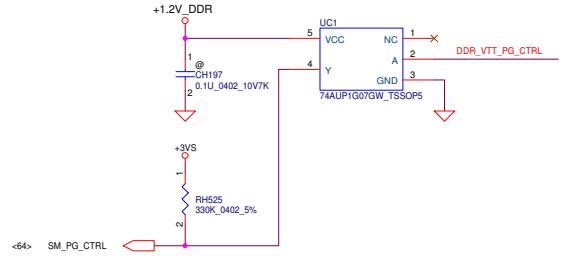


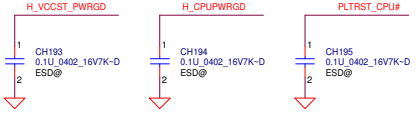
PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) *00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

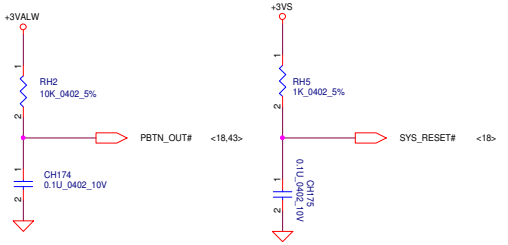


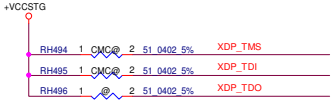
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training











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Title	CPU(3/7) CFG,XDP
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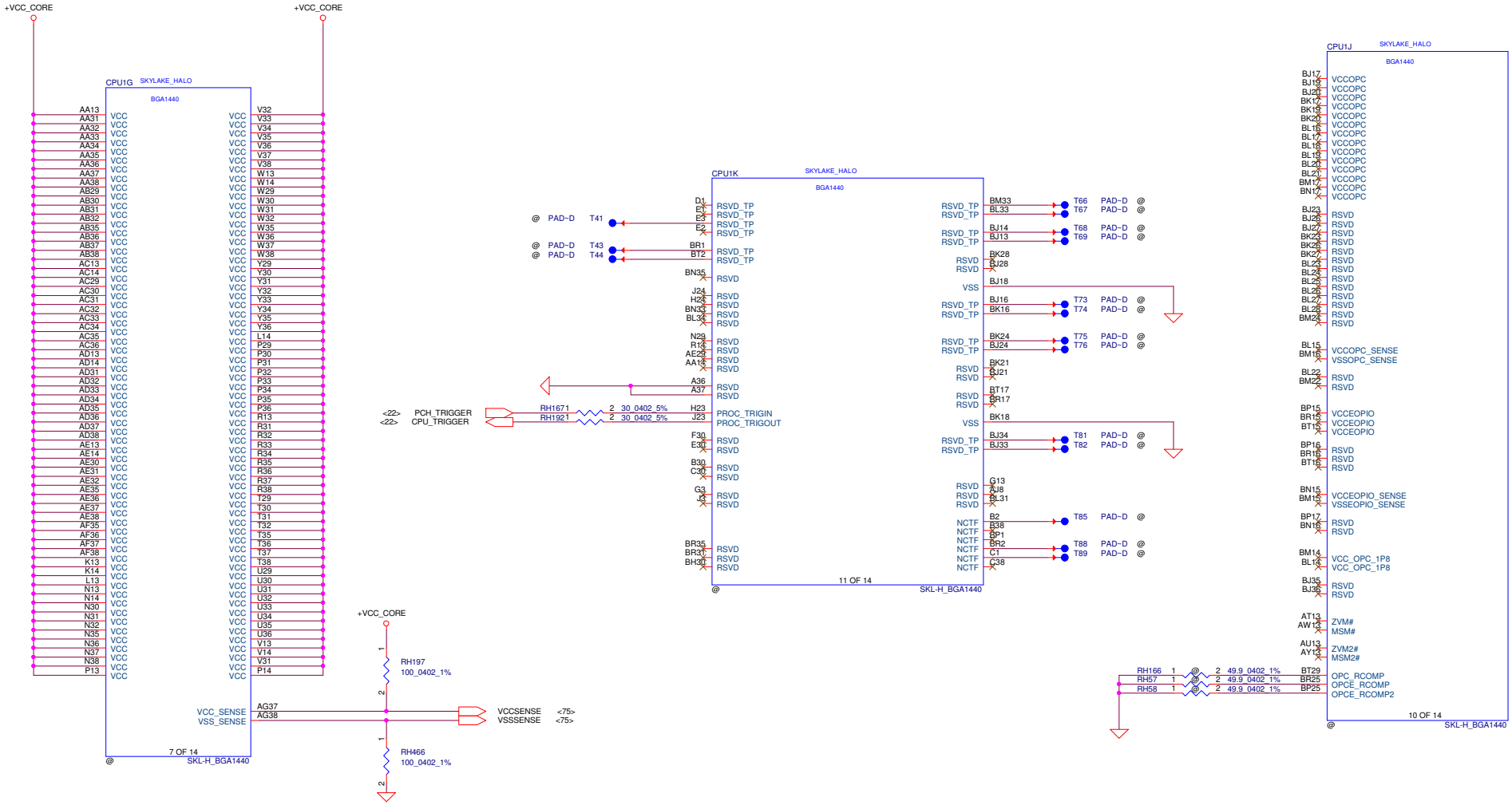

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Compal Electronics, Inc.

Title: **CPU(4/7) +VCC_CORE,RSVD**

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	LA-D751P	1.0

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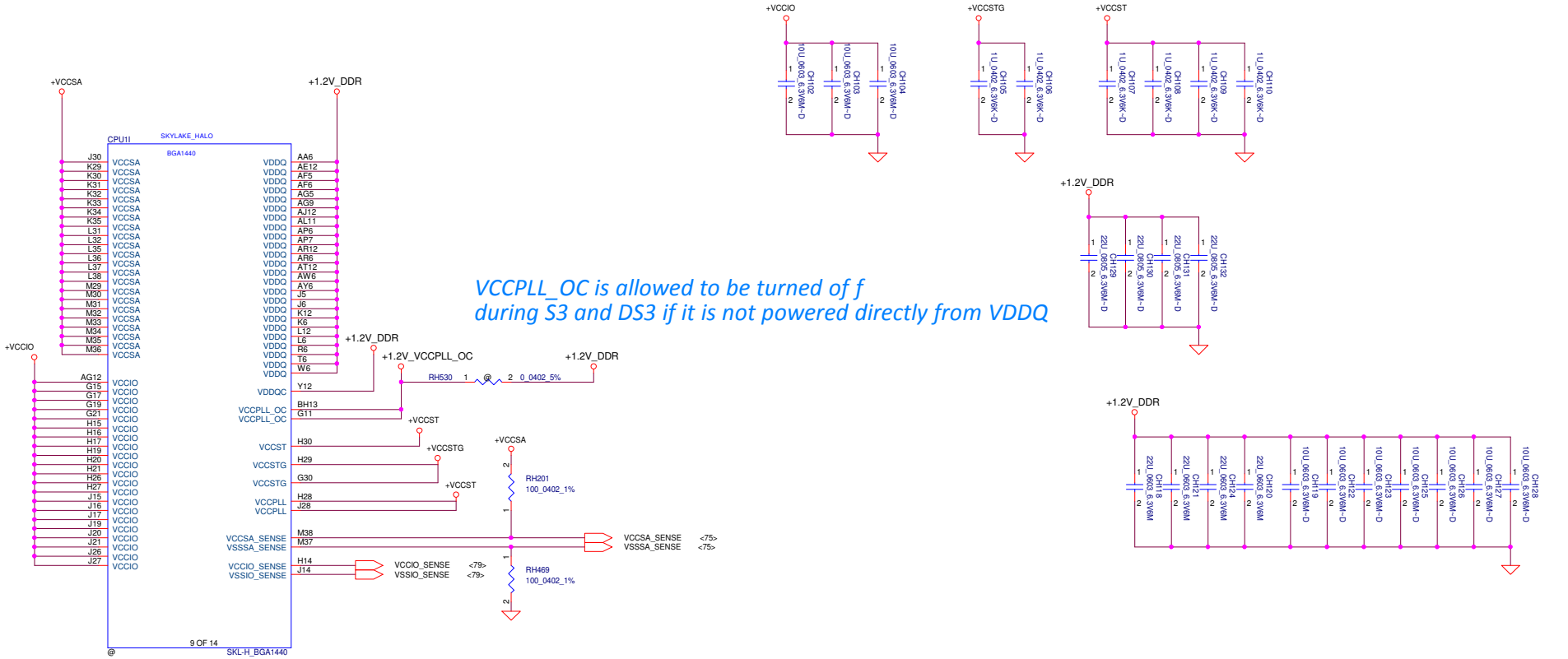

VCCPLL_OC is allowed to be turned of f
during S3 and DS3 if it is not powered directly from VDDQ

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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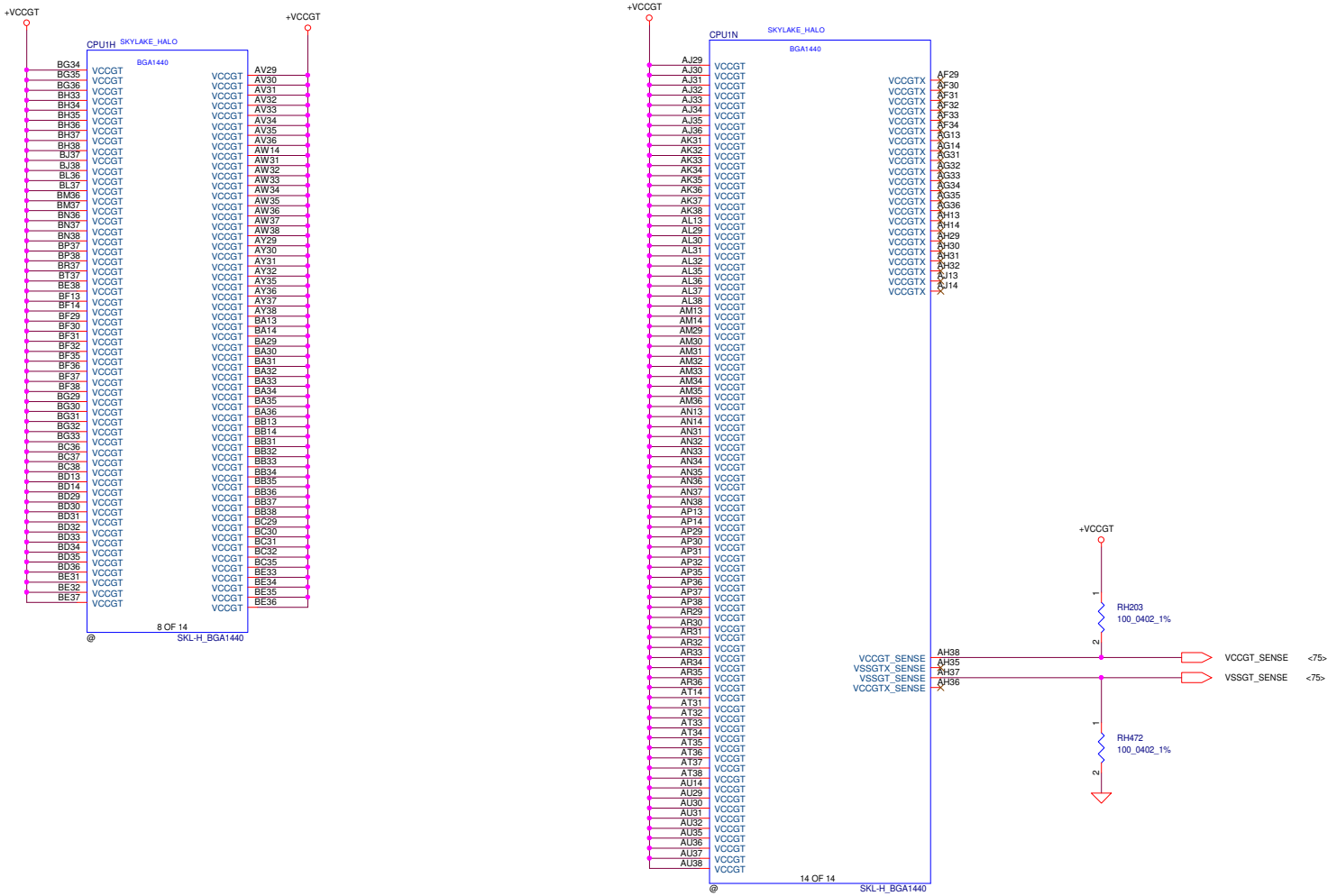
Compal Electronics, Inc.

Title: **CPU(5/7) +VCCSA,+VCCIO**

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 | Sheet 11 of 82



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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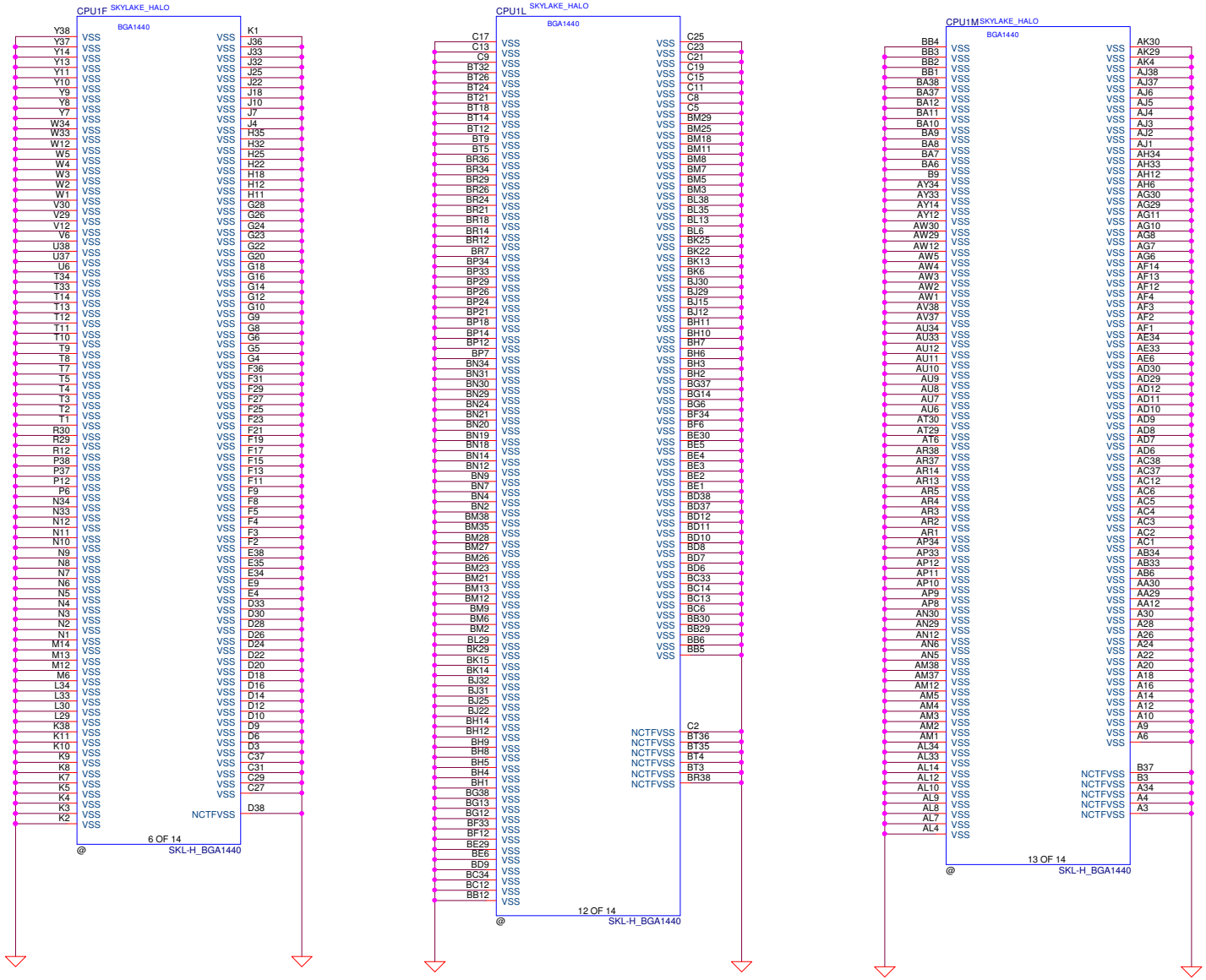
Compal Electronics, Inc.

Title: **CPU(6/7) +VCCGT**

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 | Sheet 12 of 82



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **CPU(7/7) VSS**

Size	Document Number	Rev
	LA-D751P	1.0

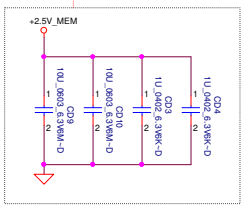
Date: Tuesday, August 16, 2016 Sheet 13 of 82

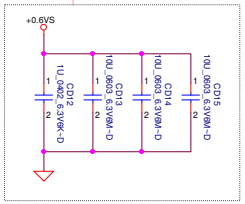
Layout Note:
Place near JDIMM1.257,259

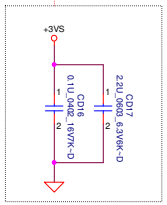
Layout Note:
Place near JDIMM1.258

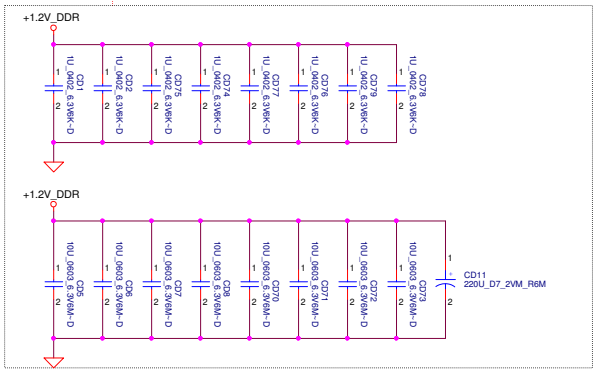
Layout Note:
Place near JDIMM1.255

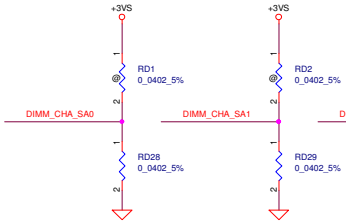
Layout Note:
Place near JDIMM1

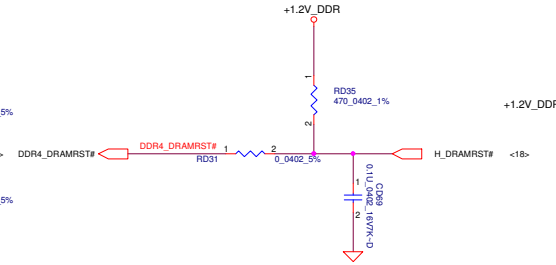


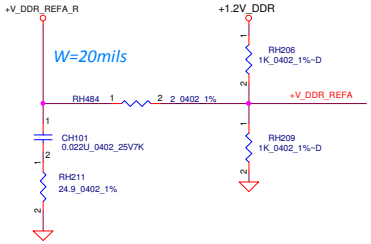


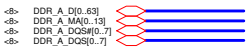






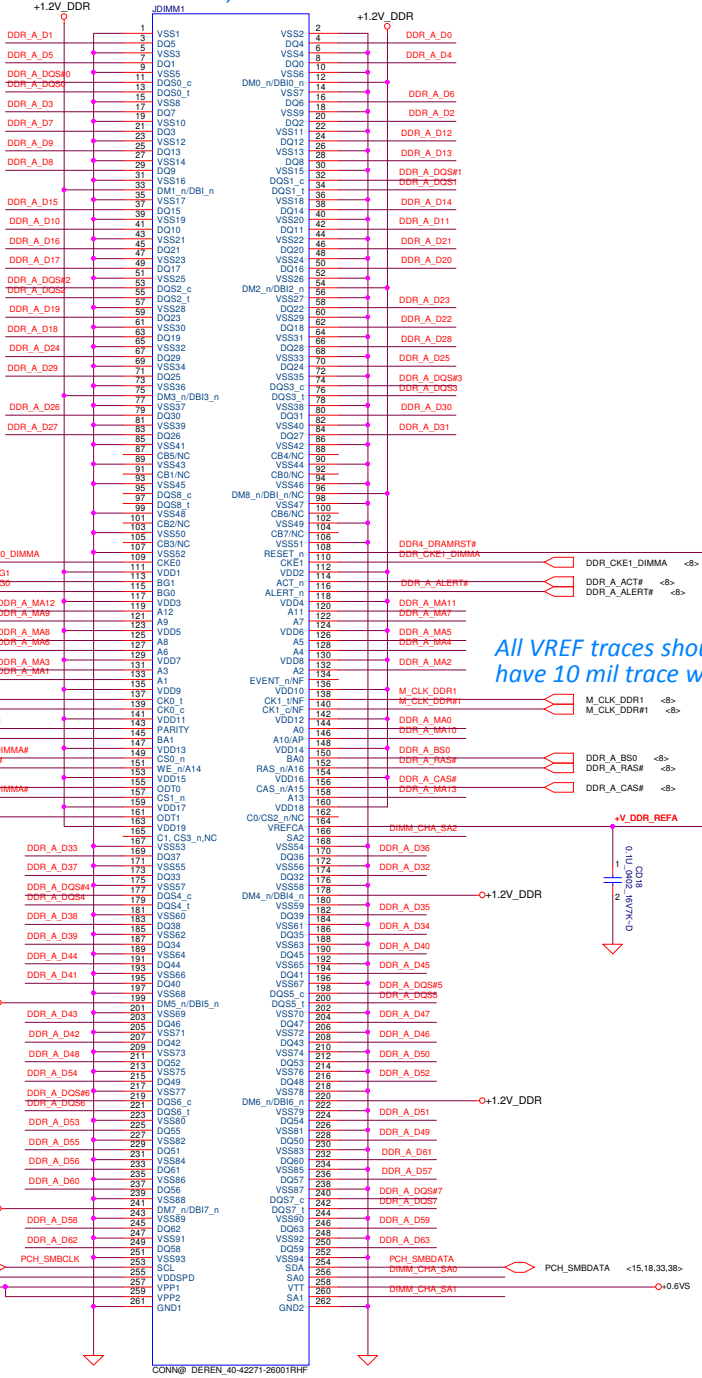






CFG Straps for Processor

4H , RVS



All VREF traces should have 10 mil trace width

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: DDR4 DIMMA,RVS

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 Sheet 14 of 82

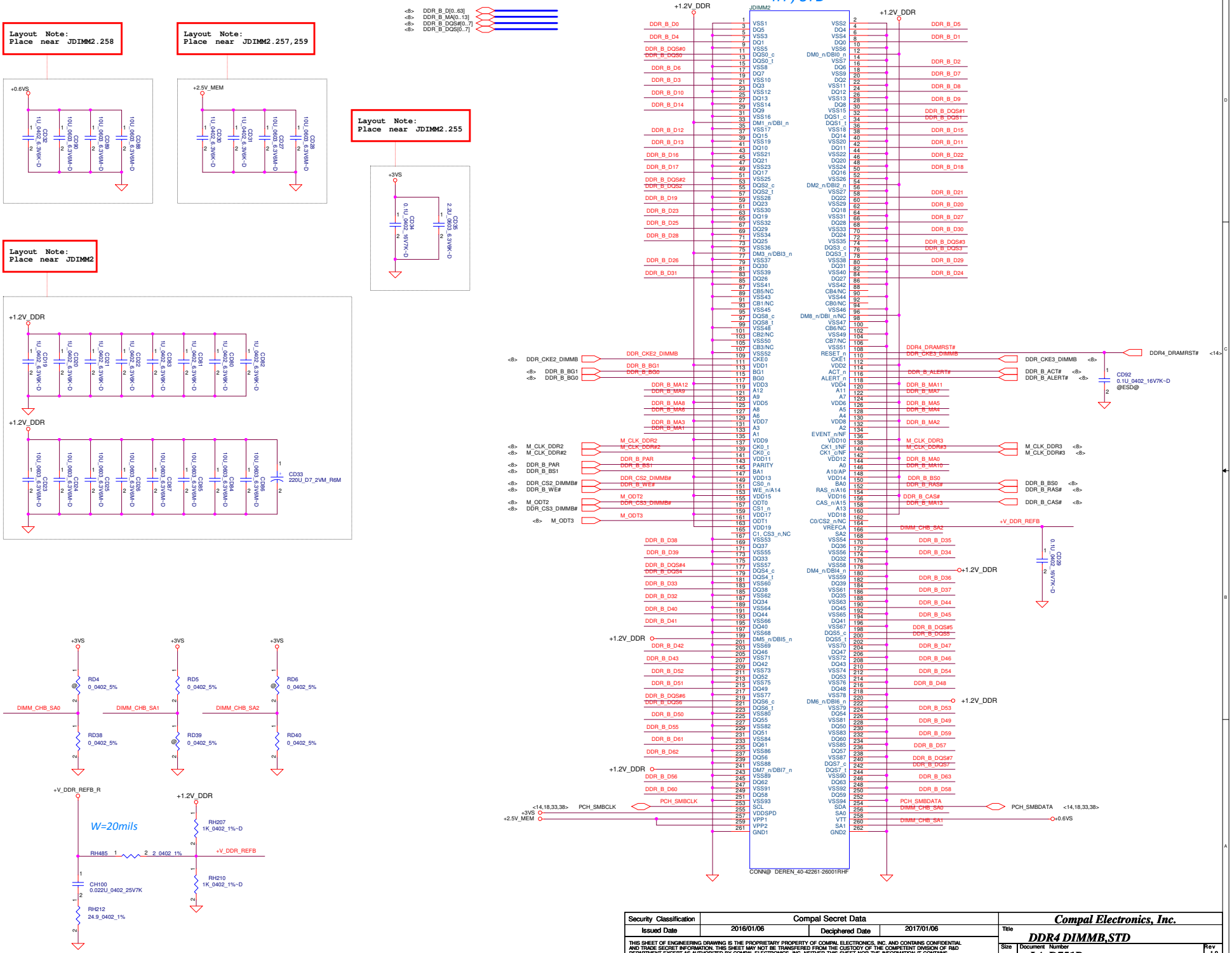
Layout Note:
Place near JDIMM2.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMM2

4H , STD



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **DDR4 DIMMB,STD**

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 | Sheet 15 of 82

UH1

S IC GLCM236 SR2CE D1 FCBGA 837P PCH-H
SA00009601L
PCHR1@

UH1

S IC GLCM236 SR2CE D1 FCBGA PCH-H A31!
SA00009602L
PCHR3@

UH1

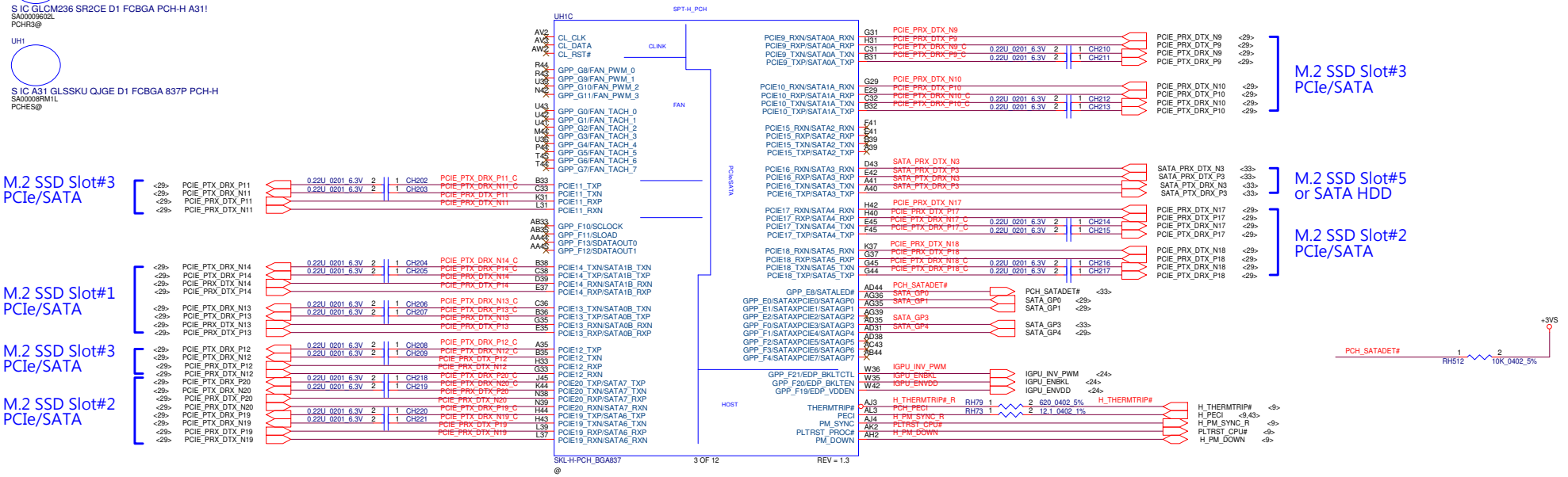
S IC A31 GLSSKU QJGE D1 FCBGA 837P PCH-H
SA00008RM1L
PCHES@

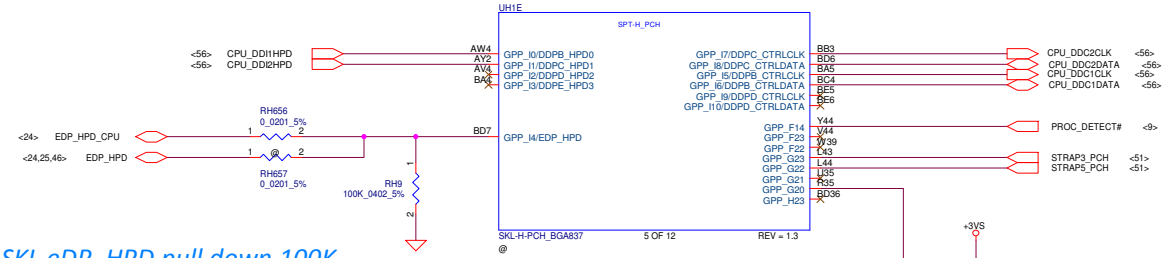
M.2 SSD Slot#3 PCIe/SATA

M.2 SSD Slot#1 PCIe/SATA

M.2 SSD Slot#3 PCIe/SATA

M.2 SSD Slot#2 PCIe/SATA





SKL eDP_HPD pull down 100K

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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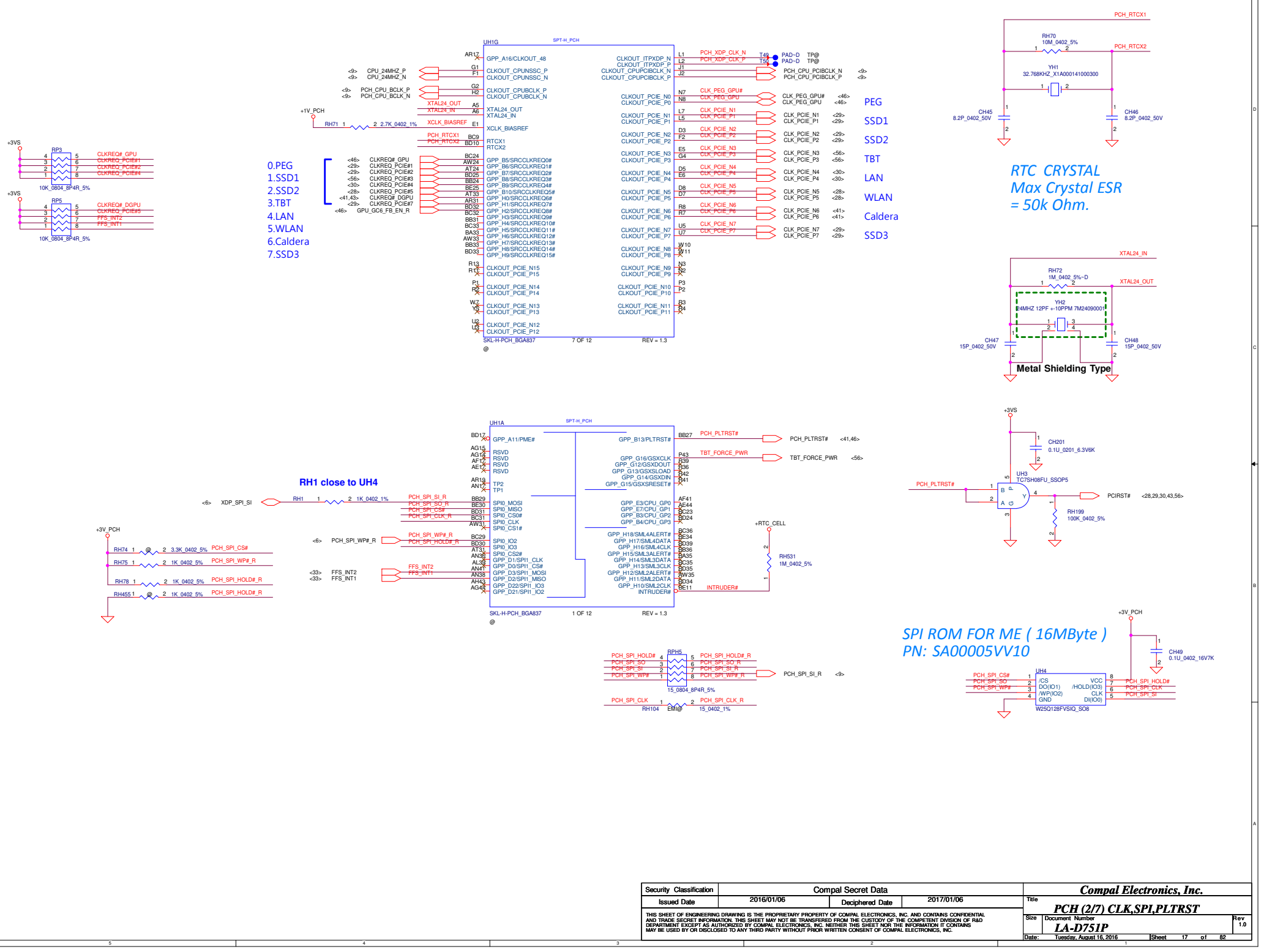
Compal Electronics, Inc.

Title: PCH (1/7) SATA,DDC,PCIE

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 | Sheet 16 of 82



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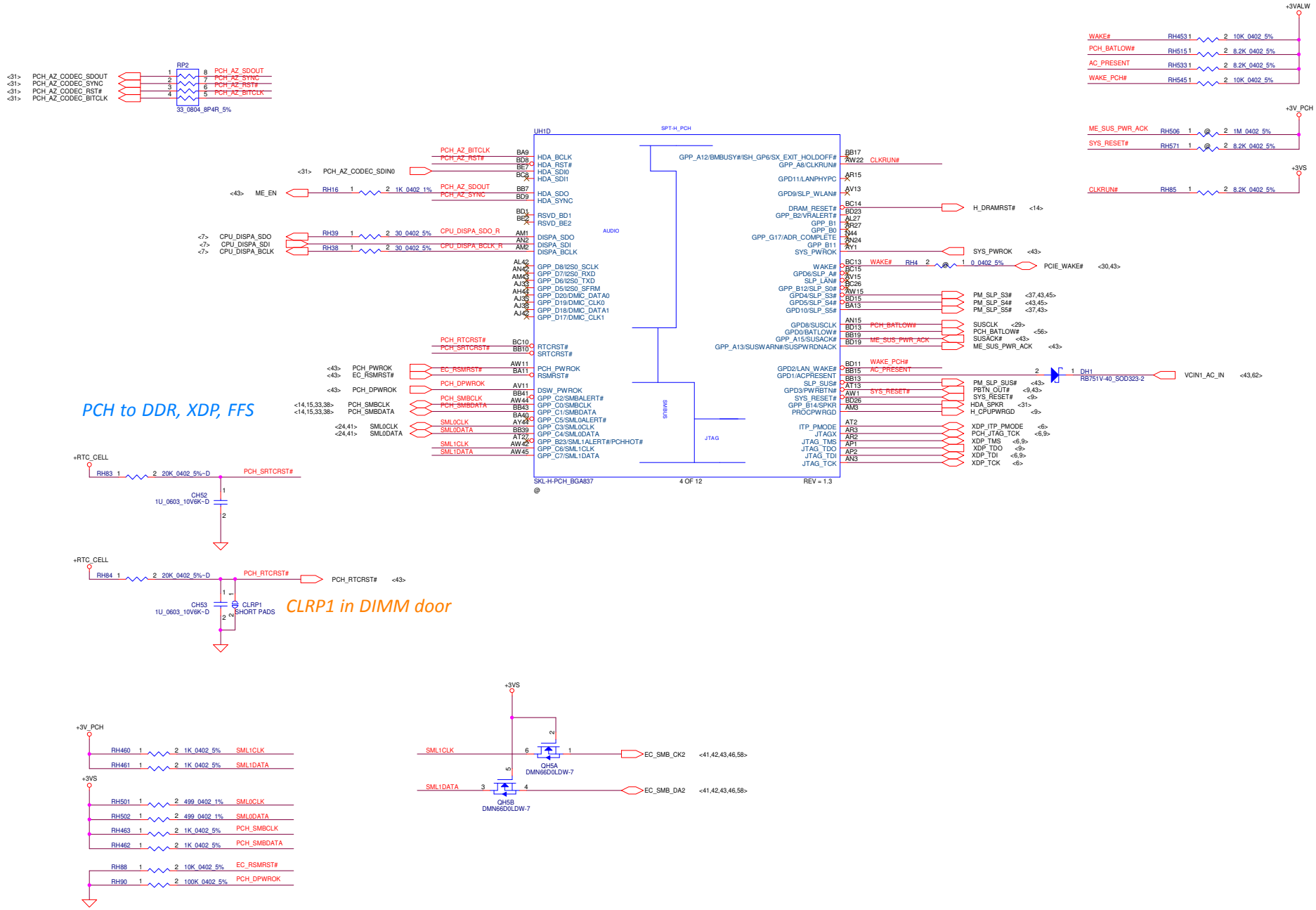
Compal Electronics, Inc.

Title: **PCH (2/7) CLK,SPI,PLTRST**

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 | Sheet 17 of 82



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **PCH (3/7) PM,HDA,SMB,JTAG**

Size	Document Number	Rev
	LA-D751P	1.0

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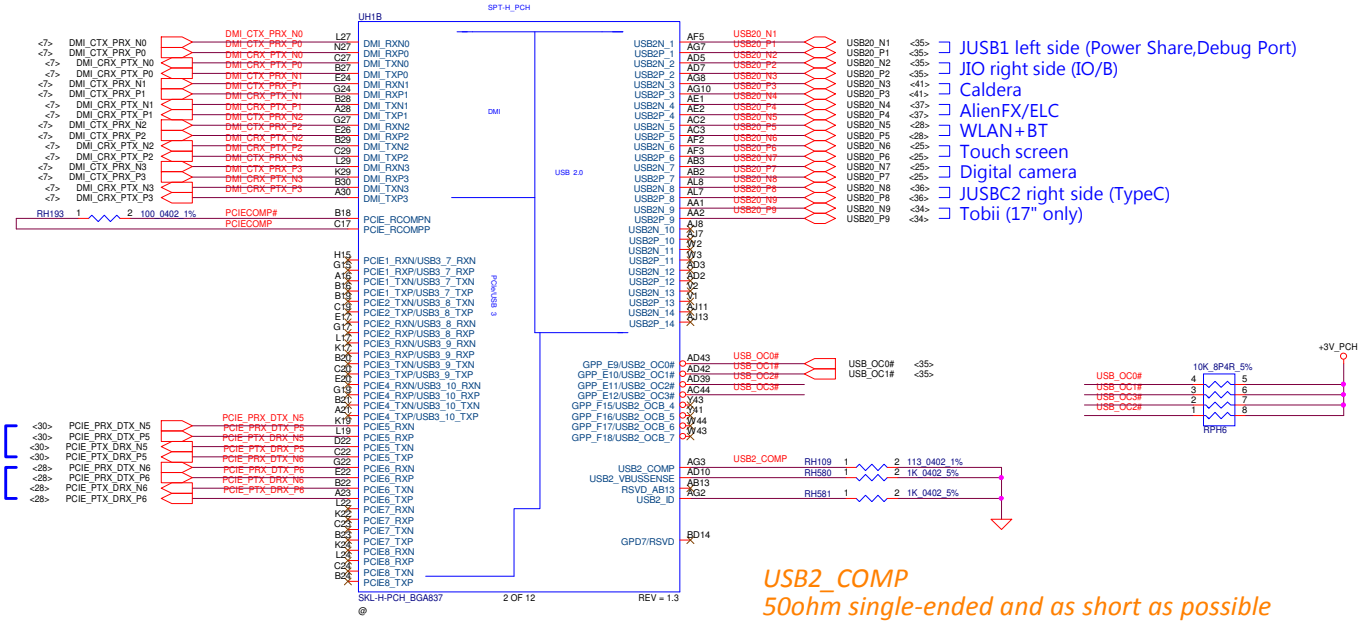

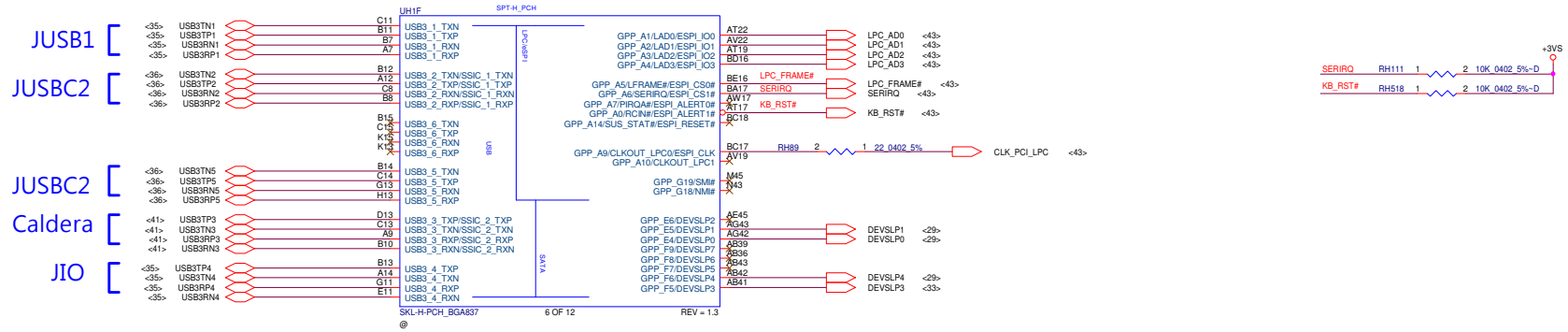

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **PCH (4/7) DMI,PCIE,USB,LPC**

Size	Document Number	Rev
	LA-D751P	1.0

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nVidia GPU_ID	N17_ID1	N17_ID0
N17EG3	H	H
N17EG2	H	L
N17EG1	L	H
N17PG1	L	L

RH25 N17EG3@ S RES 1/20W 10K +-5% 0201 SD043100280
RH27 N17EG3@ S RES 1/20W 10K +-5% 0201 SD043100280
RH25 N17EG2@ S RES 1/20W 10K +-5% 0201 SD043100280
RH28 N17EG2@ S RES 1/20W 10K +-5% 0201 SD043100280
RH26 N17EG1@ S RES 1/20W 10K +-5% 0201 SD043100280
RH27 N17EG1@ S RES 1/20W 10K +-5% 0201 SD043100280
RH26 N17PG1@ S RES 1/20W 10K +-5% 0201 SD043100280
RH28 N17PG1@ S RES 1/20W 10K +-5% 0201 SD043100280

+3VS
RH517 1 @ 2 8.2K 0402 5% BT_OFF#
RH520 1 @ 2 8.2K 0402 5% WL_OFF#
RH521 1 2 10K 0402 5% EC_SCI#
RC62 2 1 49.9K 0402 1% UART_2_CRXD_DTXD
RC63 2 1 49.9K 0402 1% UART_2_CTXD_DRXD
RC65 2 @ 1 49.9K 0402 1% UART_2_CCTS_DRTS
RH516 1 2 10K 0402 5% DGPU_PWROK
RH588 1 @ 2 10K 0402 5% VROM_SEL
RH589 1 @ 2 10K 0402 5% VROM_SEL

BOARD_ID RH21 1 NV@ 2 10K 0201 5% / RH22 1 AMD@ 2 10K 0201 5%
CPU_ID RH23 1 SKL@ 2 10K 0201 5% / RH24 1 KBL@ 2 10K 0201 5%
+3V_PCH
N17_ID1 RH25 1 @ 2 10K 0201 5% / RH26 1 @ 2 10K 0201 5%
N17_ID0 RH27 1 @ 2 10K 0201 5% / RH28 1 @ 2 10K 0201 5%
GSYNC_ID RH29 1 GSYNC@ 2 10K 0201 5% / RH30 1 NGSYNC@ 2 10K 0201 5%

UH1K SPT-H_PCH

BBS_BIT0	AT29	GPP_B22/GSPI1_MOSI	
EC_SCI#	AR29	GPP_B21/GSPI1_MISO	
VROM_SEL	AV29	GPP_B20/GSPI1_CLK	
	BC27	GPP_B19/GSPI1_CS#	
NRB_BIT	BD28	GPP_B18/GSPI0_MOSI	
	BD27	GPP_B17/GSPI0_MISO	
GC6_FB_EN	AW27	GPP_B16/GSPI0_CLK	
GC6_EVENT#	AR24	GPP_B15/GSPI0_CS#	
	AV44	GPP_C9/UART0_TXD	
	BA41	GPP_C8/UART0_RXD	
WL_OFF#	AU44	GPP_C11/UART0_CTS#	
BT_OFF#	AV43	GPP_C10/UART0_RTS#	
HDMI_HPD_PCH	AU41	GPP_C15/UART1_CTS#/ISH_UART1_CTS#	
DP_HPD_PCH	AT44	GPP_C14/UART1_RTS#/ISH_UART1_RTS#	
	AT43	GPP_C13/UART1_TXD/ISH_UART1_TXD	
EDP_MUX_PD	AU43	GPP_C12/UART1_RXD/ISH_UART1_RXD	
TBT_CIO_PLUG_EVENT#	AN43	GPP_C23/UART2_CTS#	
UART_2_CCTS_DRTS	AN44	GPP_C22/UART2_RTS#	
UART_2_CTXD_DRXD	AR39	GPP_C21/UART2_TXD	
UART_2_CRXD_DTXD	AR45	GPP_C20/UART2_RXD	
RTD3_USB_PWR_EN	AR41	GPP_C19/I2C1_SCL	
RTD3_CIO_PWR_EN	AR44	GPP_C18/I2C1_SDA	
	AR38	GPP_C17/I2C0_SCL	
	AT42	GPP_C16/I2C0_SDA	
DGPU_PWROK	AM42	GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA	
	AJ42	GPP_D23/ISH_I2C2_SCL/ISH_I2C3_SCL	

	AL44	GPP_D9	BOARD_ID
	AL36	GPP_D10	DGPU_HOLD_RST#
	AL35	GPP_D11	CPU_ID
	AJ39	GPP_D12	DGPU_PWR_EN
	AJ43	GPP_D16/ISH_UART0_CTS#	N17_ID1
	AL43	GPP_D15/ISH_UART0_RTS#	N17_ID0
	AK44	GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C2_SCL	
	AK45	GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C2_SDA	GSYNC_ID
	BC38	GPP_H20/ISH_I2C0_SCL	
	BB38	GPP_H19/ISH_I2C0_SDA	
	BD38	GPP_H22/ISH_I2C1_SCL	
	BE39	GPP_H21/ISH_I2C1_SDA	
	BC22	GPP_A23/ISH_GP5	
	BD18	GPP_A22/ISH_GP4	
	BE21	GPP_A21/ISH_GP3	
	BD22	GPP_A20/ISH_GP2	
	BD21	GPP_A19/ISH_GP1	
	BB22	GPP_A18/ISH_GP0	CLKDET#
	BC19	GPP_A17/ISH_GP7	DGPU_PRSNT#

SKL-H-PCH_BGA837 11 OF 12 REV = 1.3

DGPU_HOLD_RST# <46>
DGPU_PWR_EN <43,49>
XMP2 <64>
XMP1 <64>
RH135 10K_0402_5%

+3VS DGPU_PWR_EN RH537 1 2 10K 0201 5%
+3V_PCH CLKDET# RH558 1 @ 2 10K 0201 5%

+3V_PCH RH130 1 @ 2 4.7K 0402 5%-D BBS_BIT0

Boot BIOS Strap Bit (internal PD)	
HIGH	LPC
LOW(DEFAULT)	SPI

+3V_PCH RH524 1 @ 2 4.7K 0402 5%-D NRB_BIT

NO REBOOT mode (internal PD)	
HIGH	Enable
LOW(DEFAULT)	Disable

+5VALW
JWDB ACES_88266-04001 CONN@
UART_2_CTXD_DRXD
UART_2_CRXD_DTXD

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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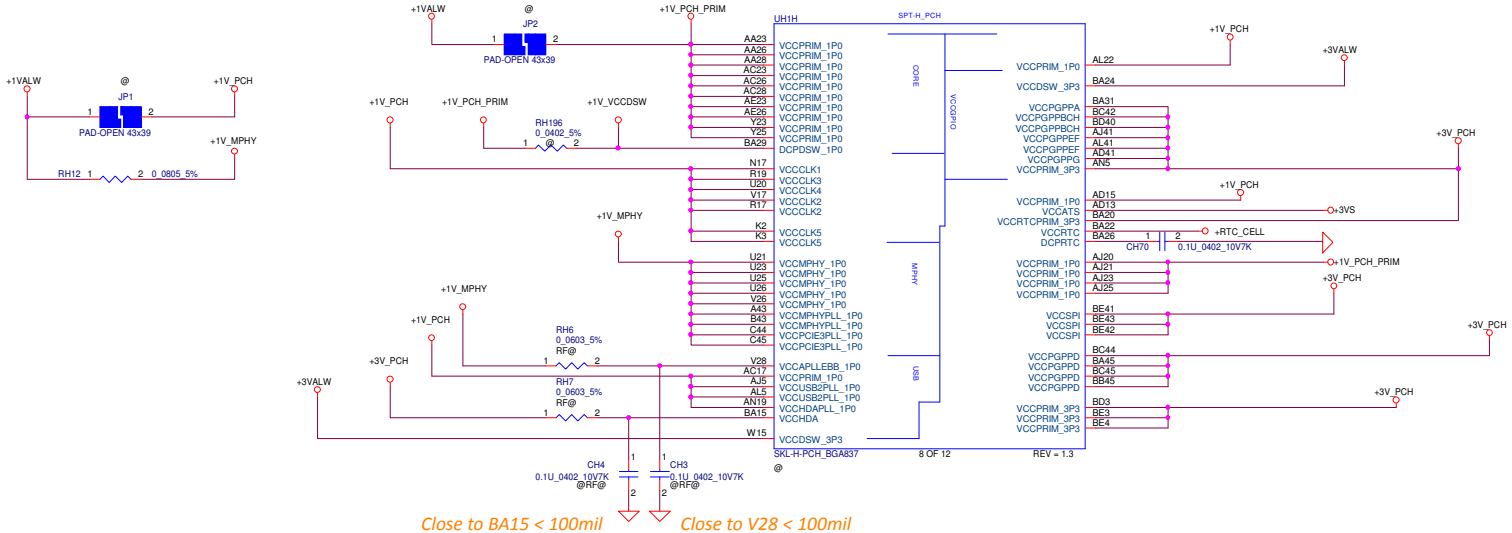
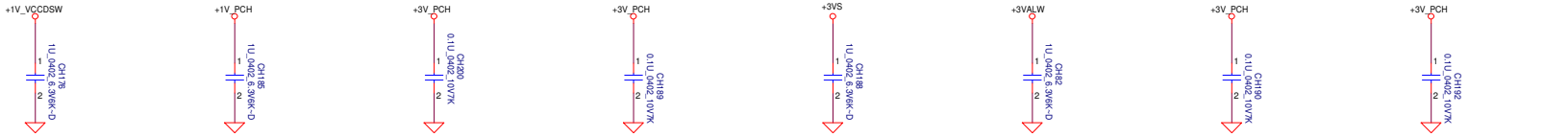
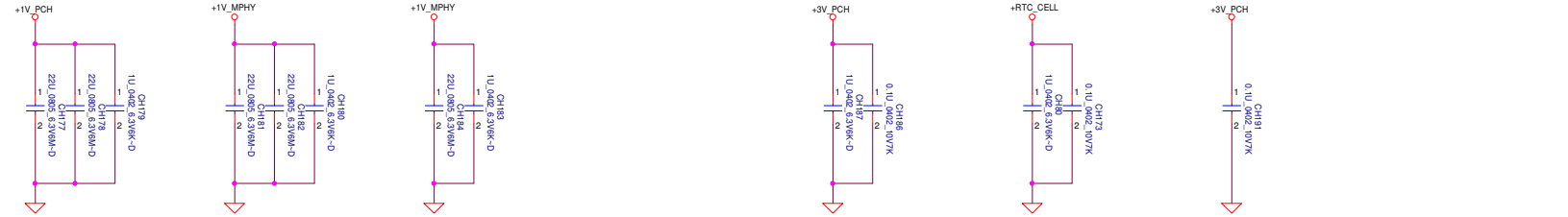
Compal Electronics, Inc.
Title: PCH (5/7) I2C,GPIO
Size: Document Number: LA-D751P Rev: 1.0
Date: Tuesday, August 16, 2016 Sheet 20 of 82



Close to BA15 < 100mil Close to V28 < 100mil



Close to BA29 Close to AC17 Close to BA15 Close to AN5 Close to AD13 Close to W15 Close to AD41 Close to BC42,BD40



Close to K2,K3 Close to A43,B43 Close to U21,U23,U25,U26,V26 Close to BA20 Close to BA22 Close to AJ41,AL41

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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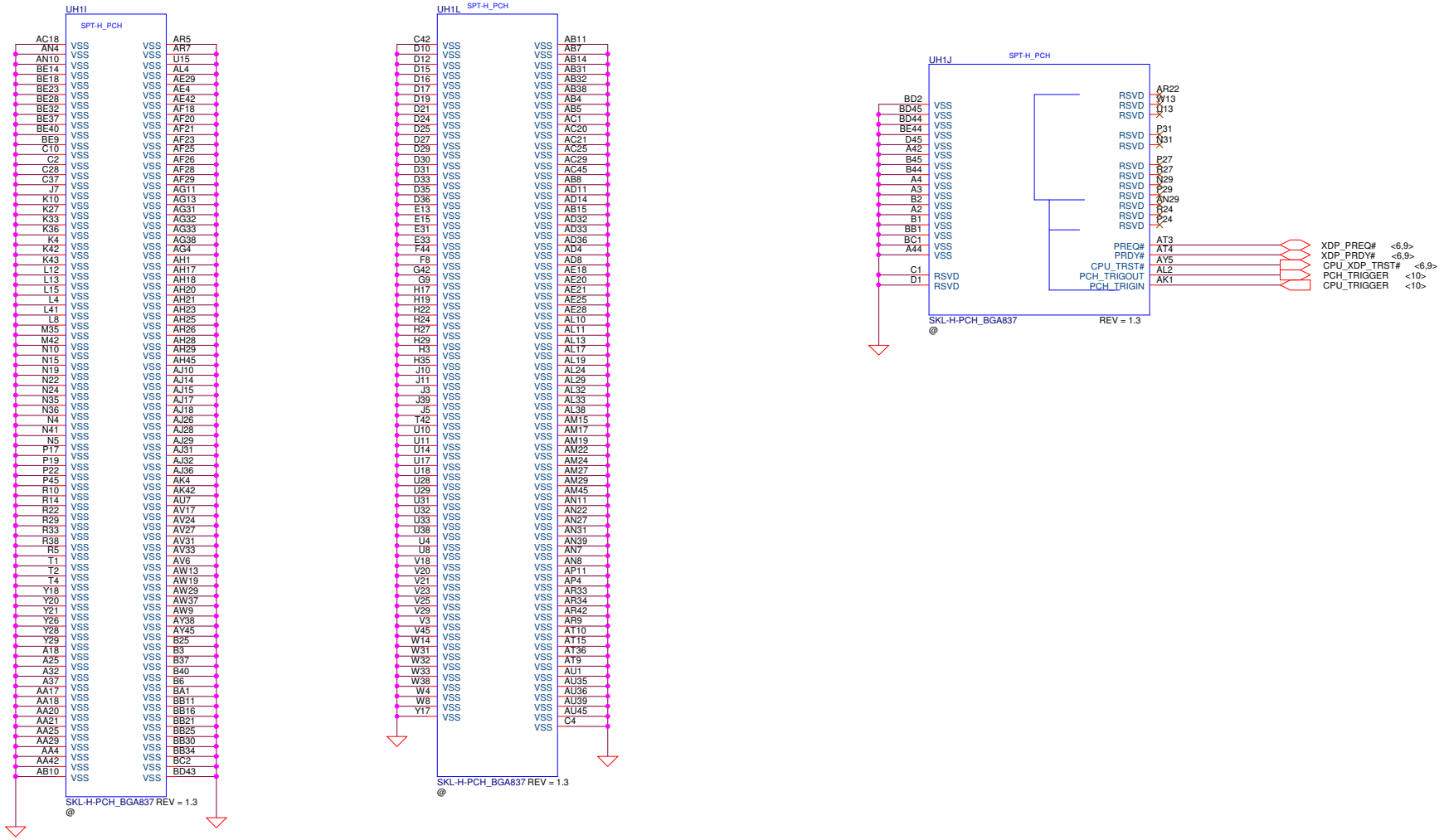
Compal Electronics, Inc.

Title: **PCH (6/7) PWR**

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 Sheet 21 of 82



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **PCH (7/7) VSS**

Size	Document Number	Rev
	LA-D751P	1.0

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Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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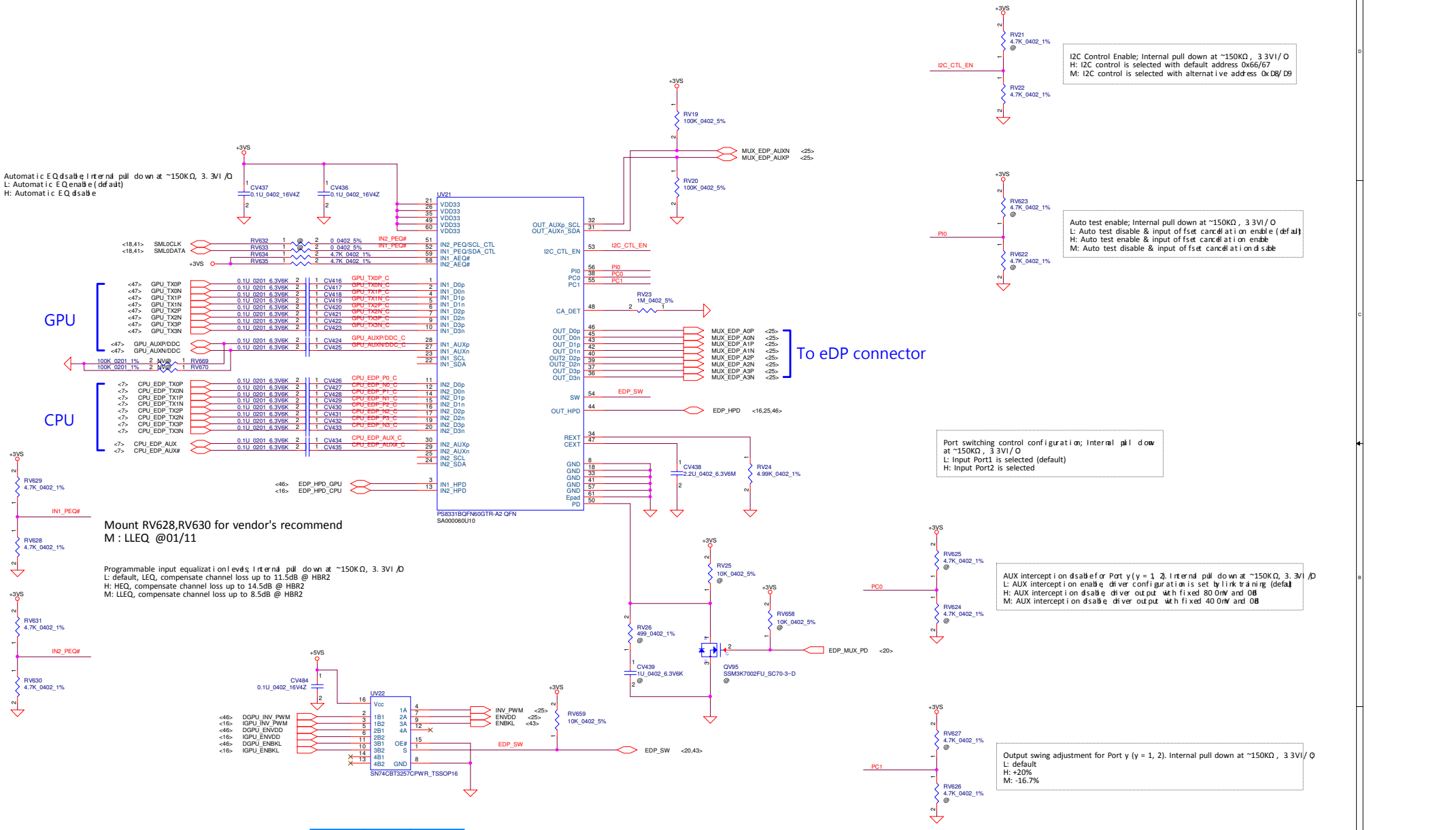
Compal Electronics, Inc.

Title: **Reversed**

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 | Sheet 23 of 82



S1	OE	output	function
L	L	A=B1	DGPU
H	L	A=B2	IGPU
X	H		

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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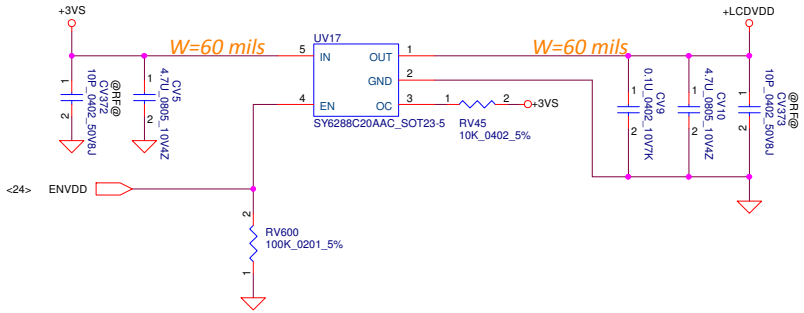
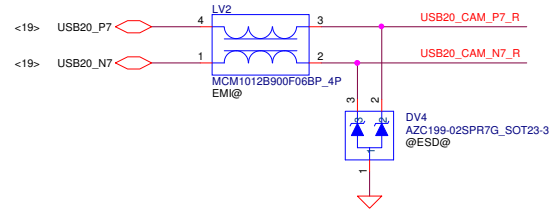
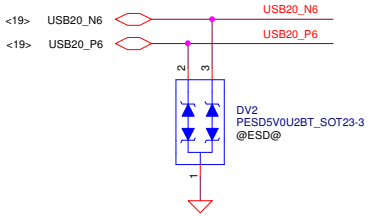
Compal Electronics, Inc.	
Title	eDP MUX PS8331B
Size	Document Number: LA-D751P
Rev	1.0
Date:	Tuesday, August 16, 2016
Sheet	24 of 82

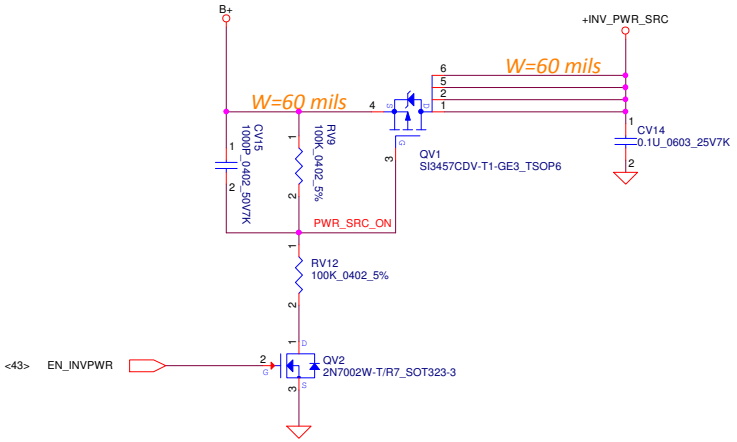
LCD power control



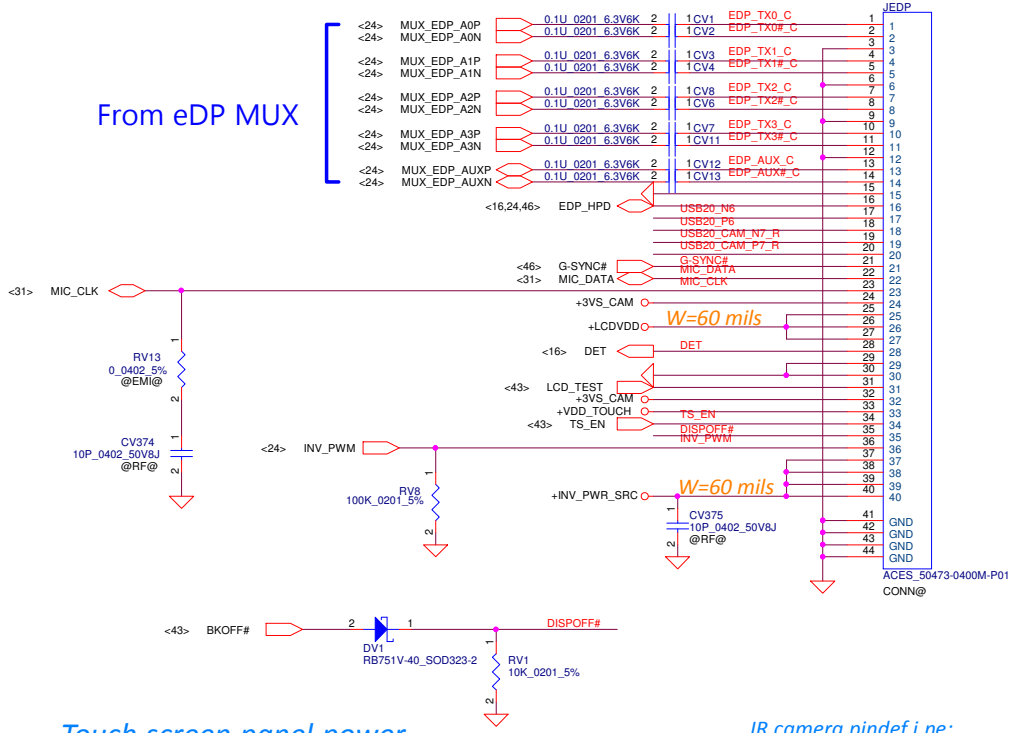




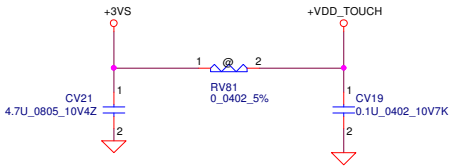
LCD backlight power control



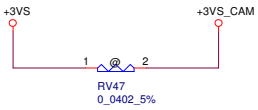
eDP connector

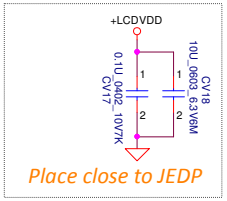


Touch screen panel power



Camera power





IR camera pindef i ne:
IR_LED+
IR_LED+
IR_LED+/NC
IR_LED-/DET , connect to PCH GPIO
IR_LED-
IR_LED-
Diglog_loop , connect to PCH GPIO
DGND
D+
D-
USB3V3
MIC_SIG
MIC_CLK
DGND

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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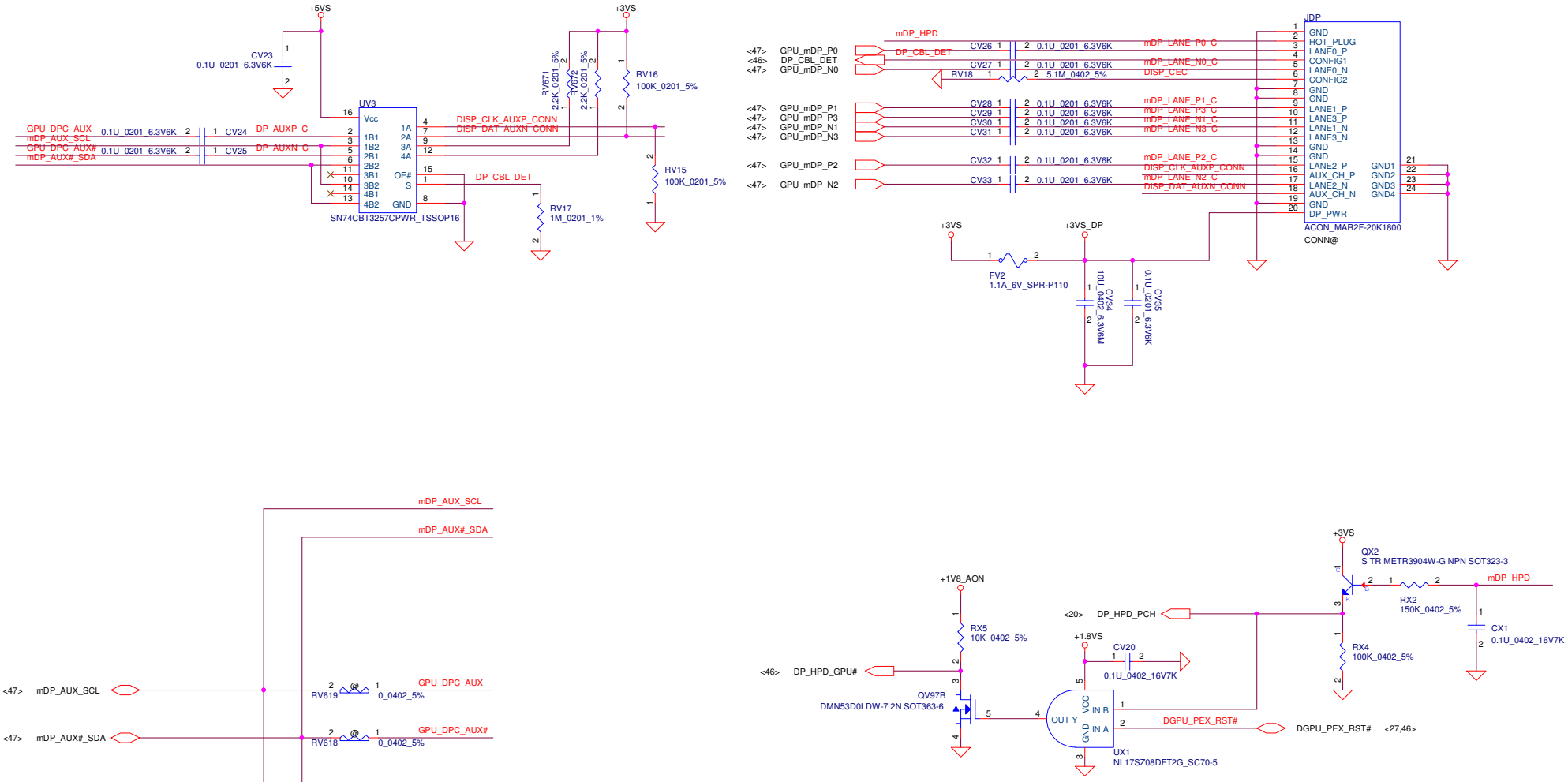
Compal Electronics, Inc.

Title: **eDP/Camera/TS**

Size | Document Number: **LA-D751P** | Rev: 1.0

Date: Tuesday, August 16, 2016 | Sheet 25 of 82



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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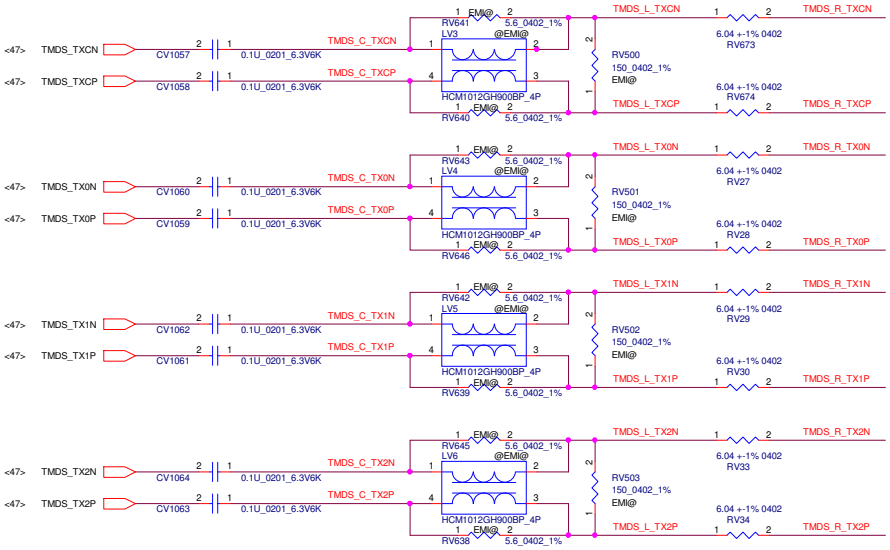
Compal Electronics, Inc.

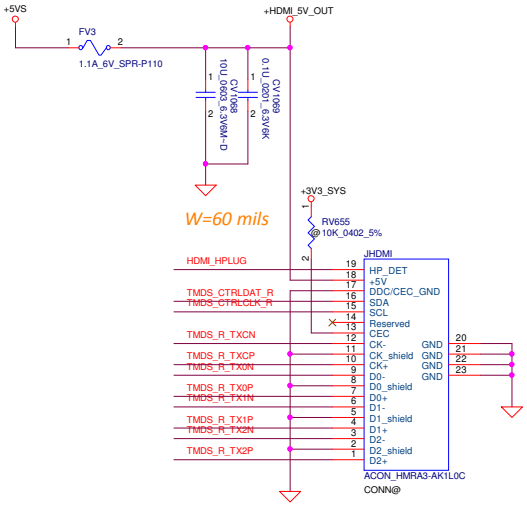
Title: **Mini DP**

Size | Document Number: **LA-D751P** | Rev: 1.0

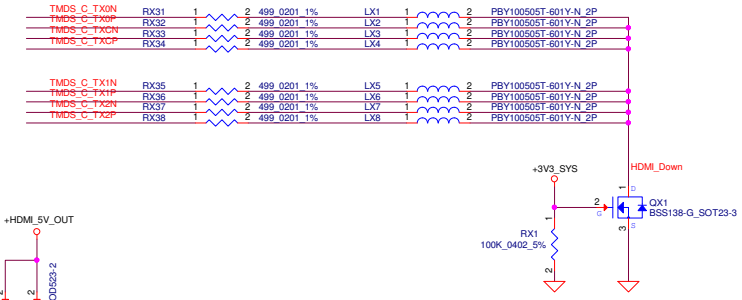
Date: Tuesday, August 16, 2016 | Sheet 26 of 82

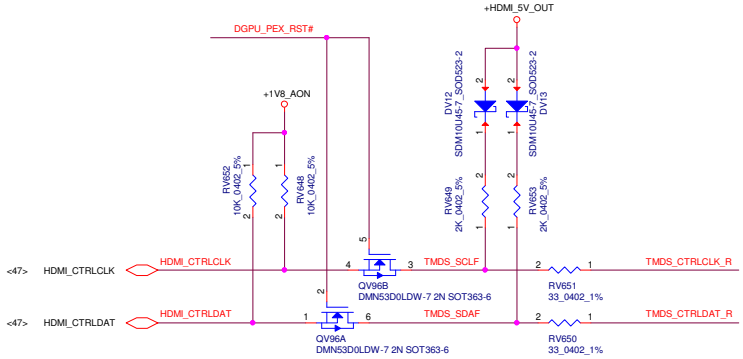
Reserve LV3,LV4,LV5,LV6 co-lay with EMI solut i on @01/12



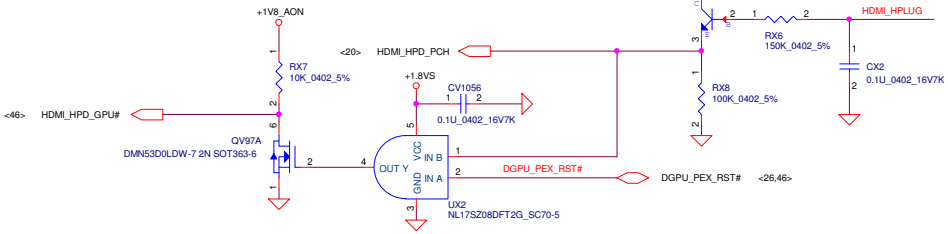


W=60 mils





To GPU



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **HDMI**

Size | Document Number: **LA-D751P** | Rev: 1.0

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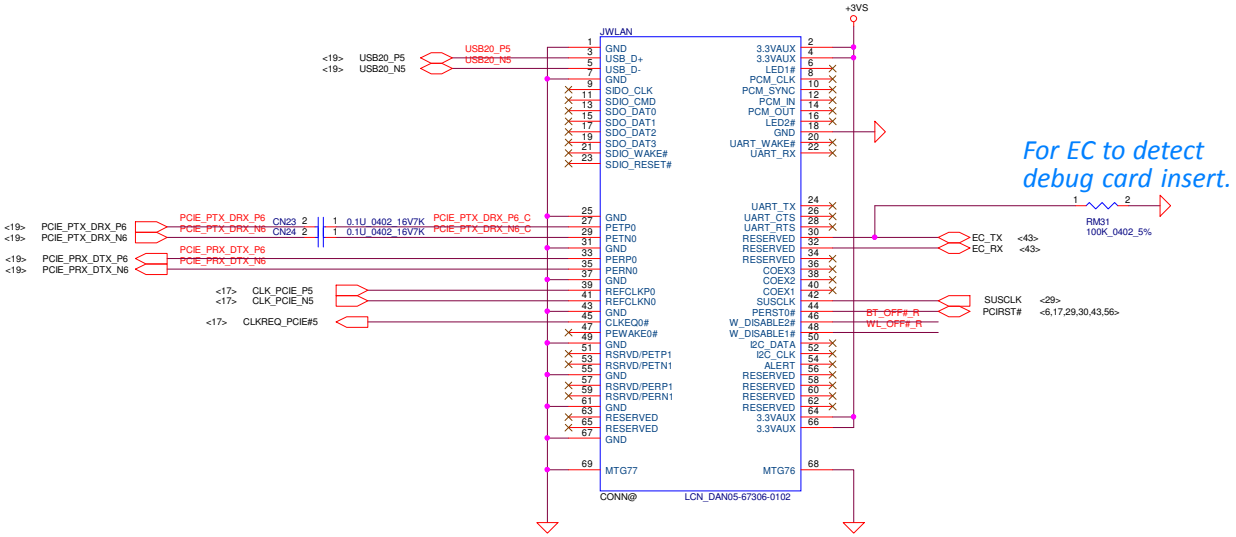
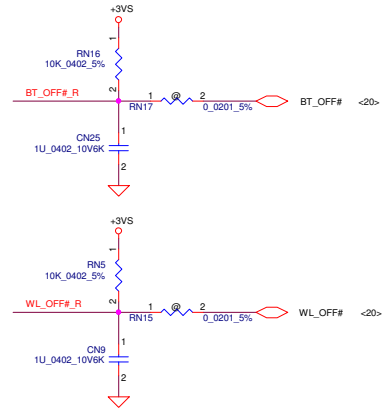
M.2 2230 slot(type E)

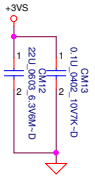


For EC to detect debug card insert.

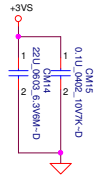


Prevent backdriver from +3VS_WLAN_NGFF to +3VS

closed to pin 2, 4



closed to pin 64, 66



WLAN power control

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **NGFF WLAN/BT**

Size	Document Number	Rev
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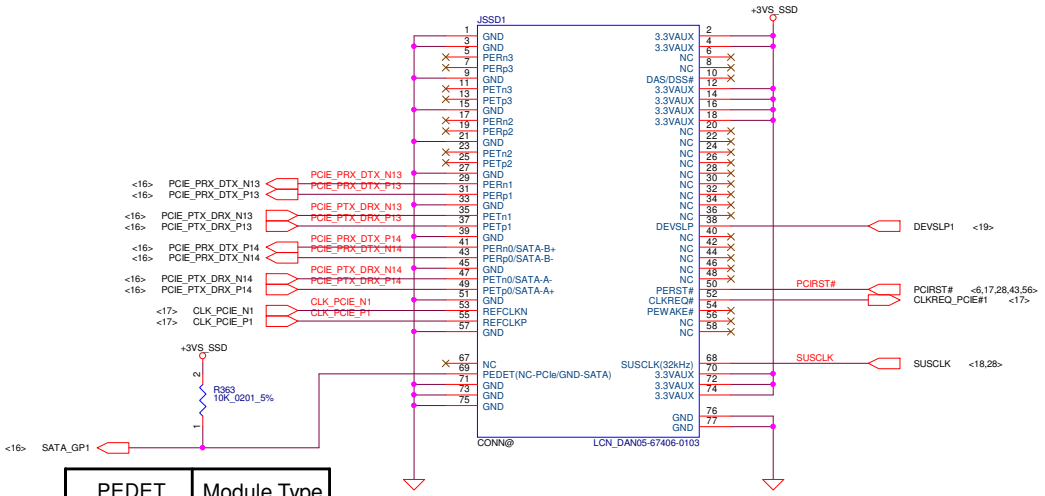
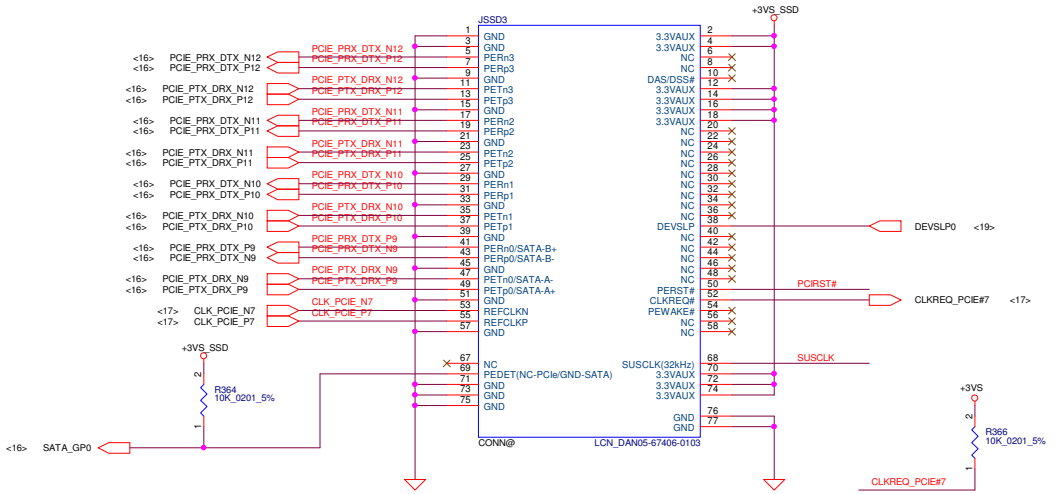
PCIe/SATA SSD
NGFF Slot_1 Key M

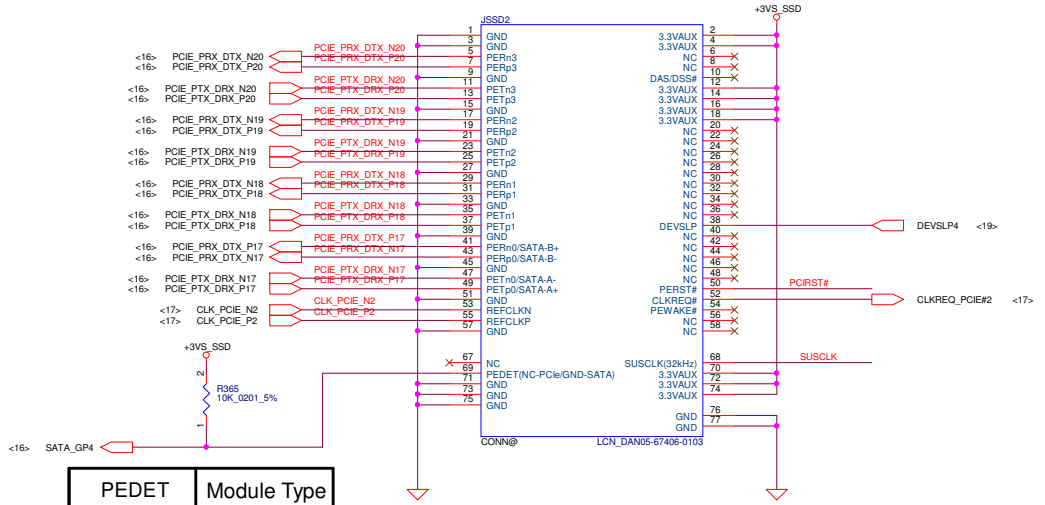


PEDET	Module Type
0	SATA
1	PCIe

PCIe/SATA SSD
NGFF Slot_3 Key M

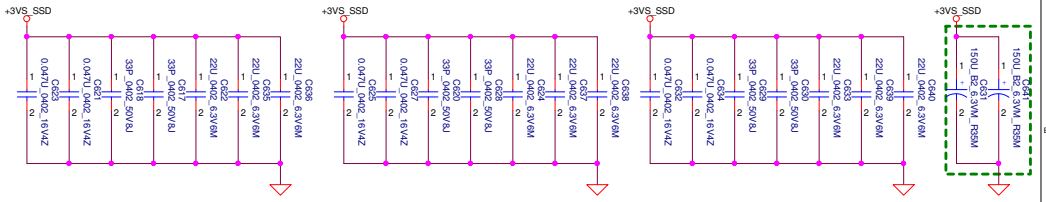


PCIe/SATA SSD
NGFF Slot_2 Key M

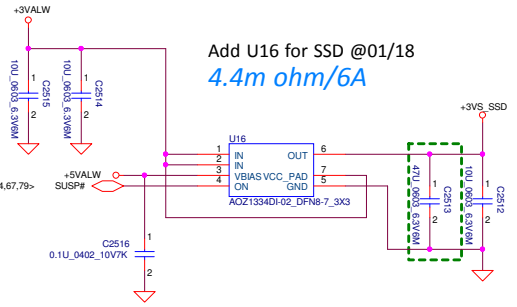


PEDET	Module Type
0	SATA
1	PCIe

JSSD1 JSSD2 JSSD3



Delete C619,C626 @12/29
C622,C624 from 0805 to 0402 @01/08
Add 22U C635,C636,C637,C638,C639,C640 @01/08



Add U16 for SSD @01/18
4.4m ohm/6A

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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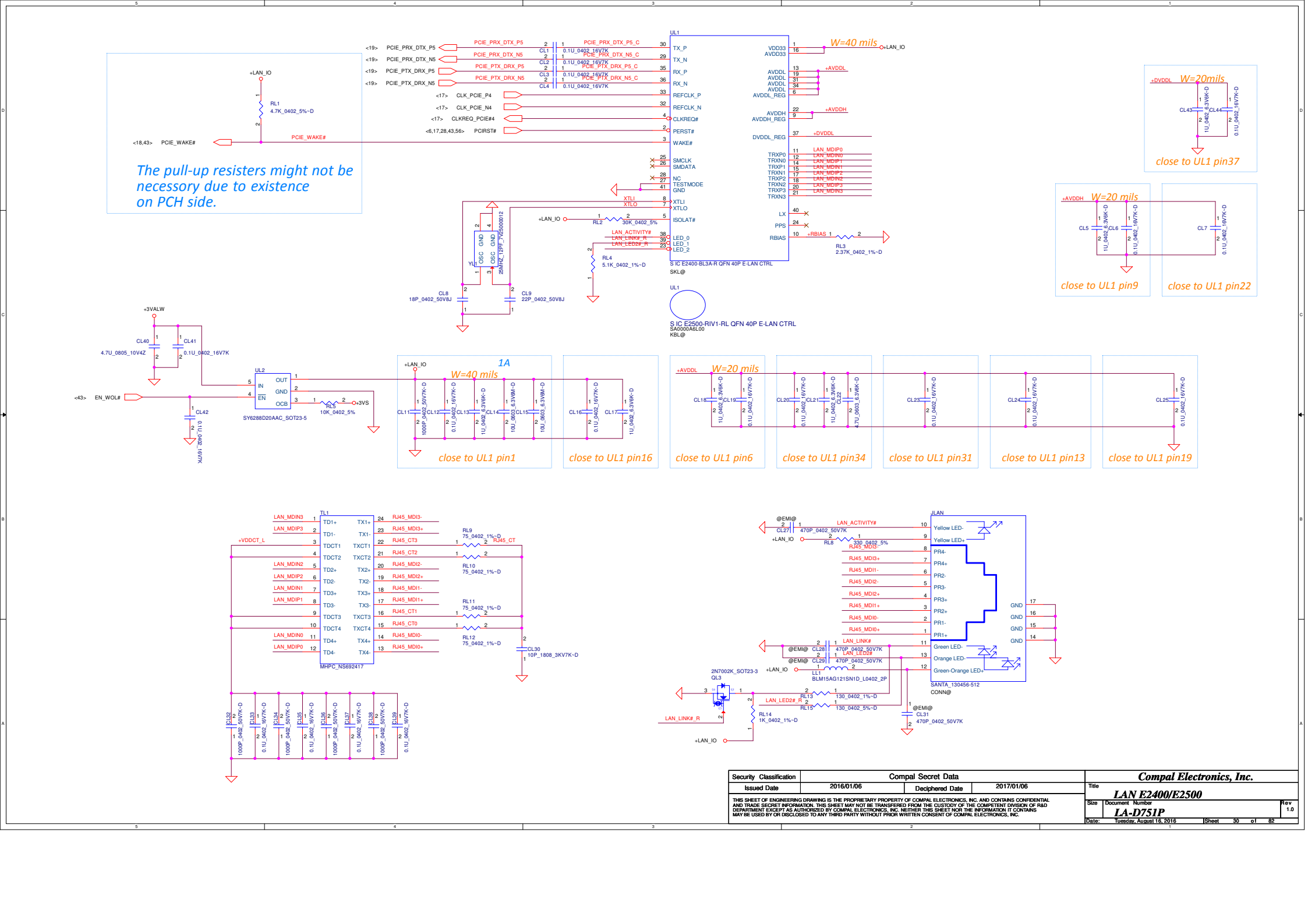
Compal Electronics, Inc.

Title: **NGFF SSD**

Size: | Document Number: **LA-D751P** | Rev: 1.0

Date: Friday, September 02, 2016 | Sheet 29 of 82



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **LAN E2400/E2500**

Size	Document Number	Rev
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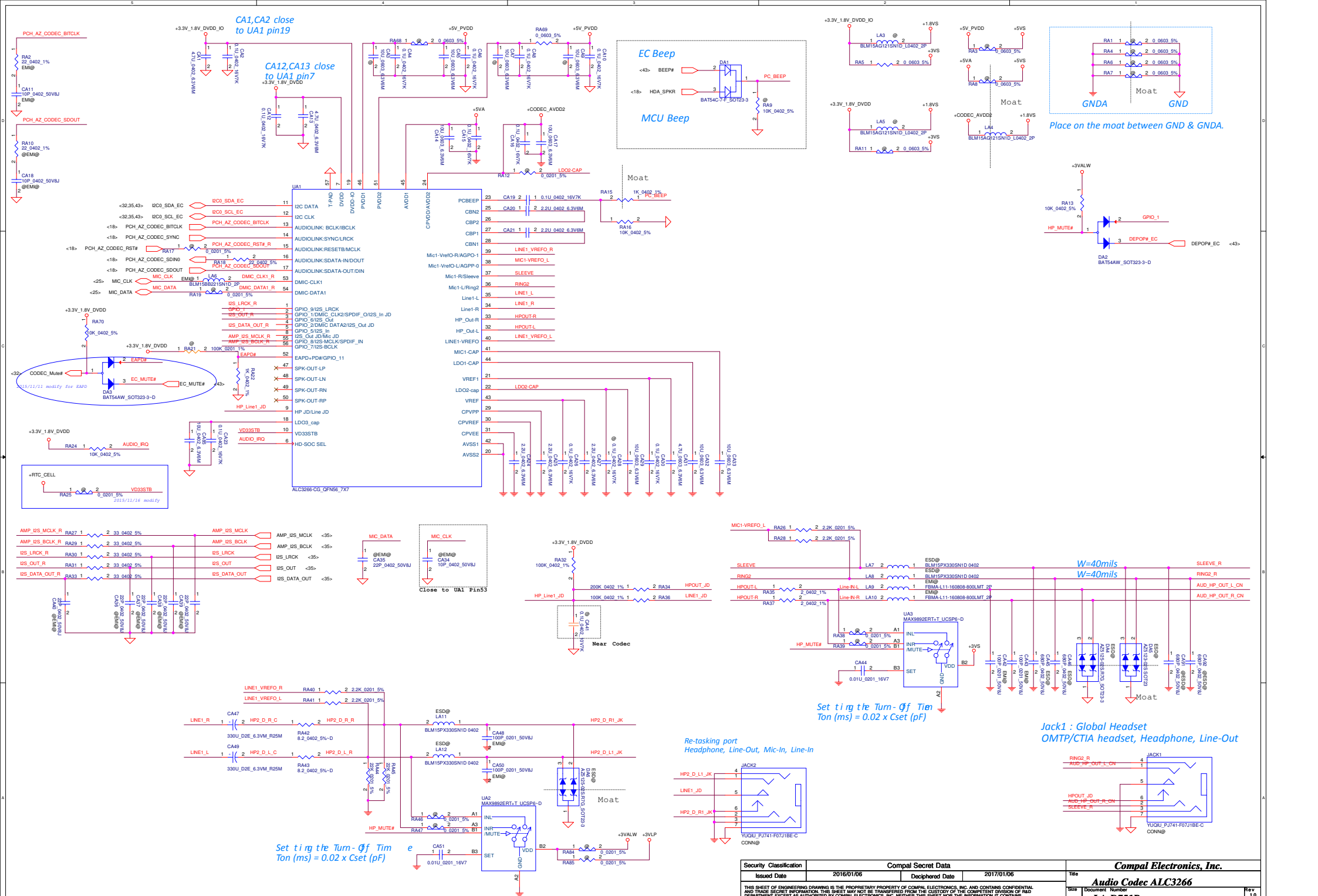

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **Audio Codec ALC3266**

Size: | Document Number: **LA-D751P** | Rev: 1.0

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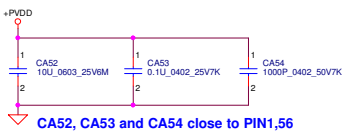
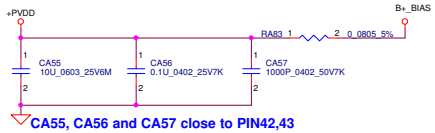
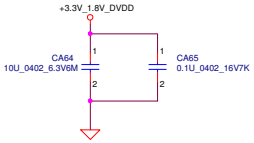
SMART AMP



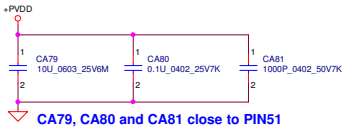
CA52, CA53 and CA54 close to PIN1,56



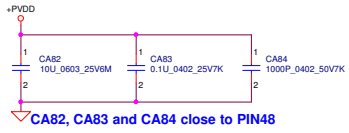
CA55, CA56 and CA57 close to PIN42,43



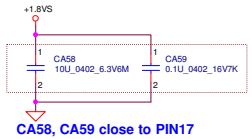
CA64, CA65 close to PIN16



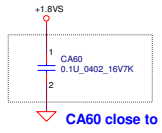
CA79, CA80 and CA81 close to PIN51



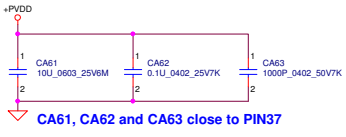
CA82, CA83 and CA84 close to PIN48



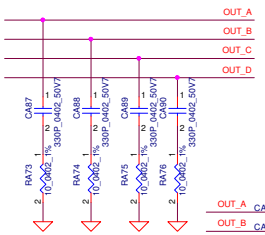
CA58, CA59 close to PIN17

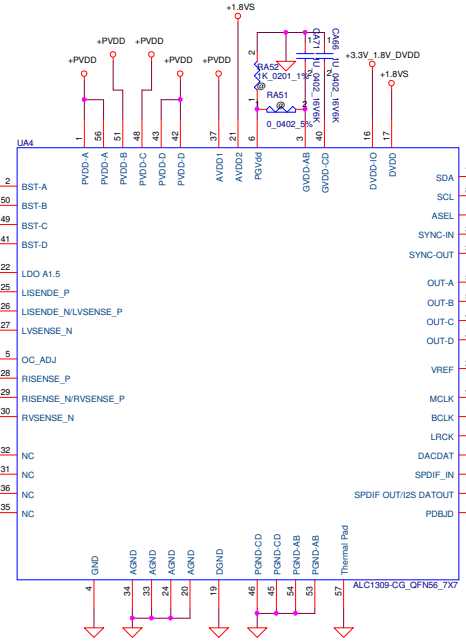


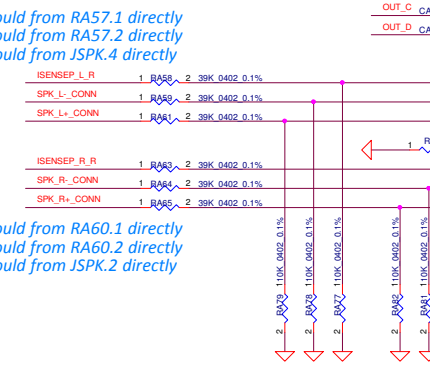
CA60 close to PIN21



CA61, CA62 and CA63 close to PIN37

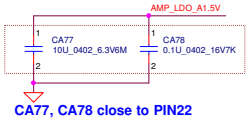




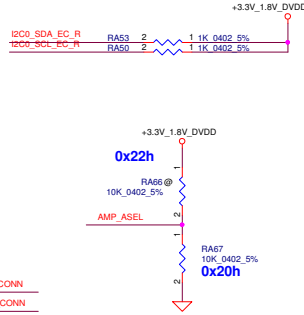


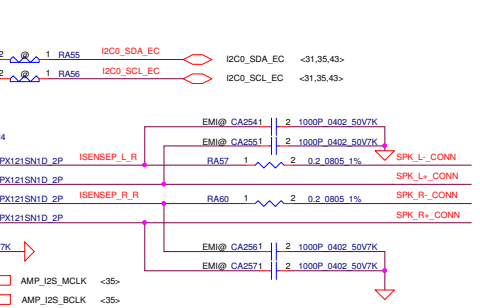
RA58.1 should from RA57.1 directly
RA59.1 should from RA57.2 directly
RA61.1 should from JSPK.4 directly

RA63.1 should from RA60.1 directly
RA64.1 should from RA60.2 directly
RA65.1 should from JSPK.2 directly



CA77, CA78 close to PIN22

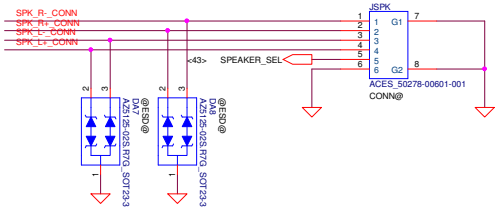




Int. Speaker Conn.

40 mils = For 4 ohm 3W Speaker

Close to UA1 Pin42,43,44,45



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40 mil
Speaker 8 ohm : 20 mil

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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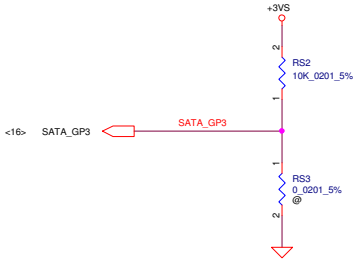
Compal Electronics, Inc.

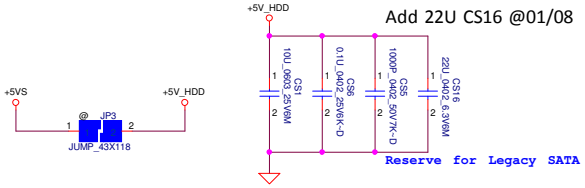
Title: Audio Amplifier ALC1309

Size: | Document Number: LA-D751P | Rev: 1.0

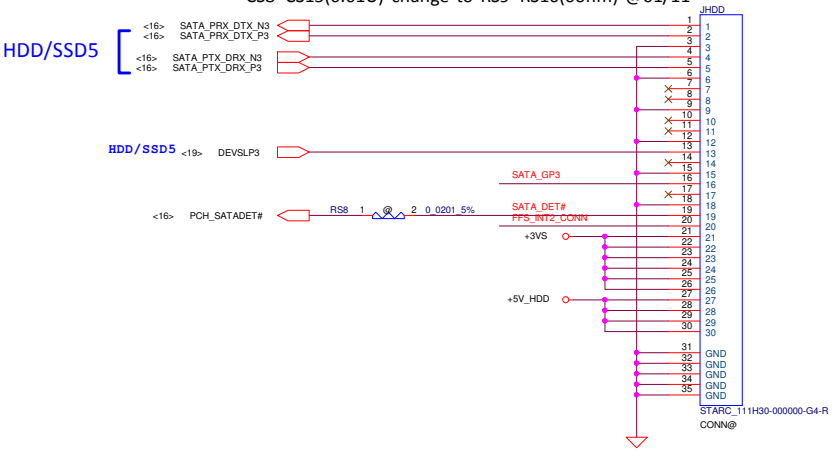
Date: Tuesday, August 16, 2016 | Sheet 32 of 82

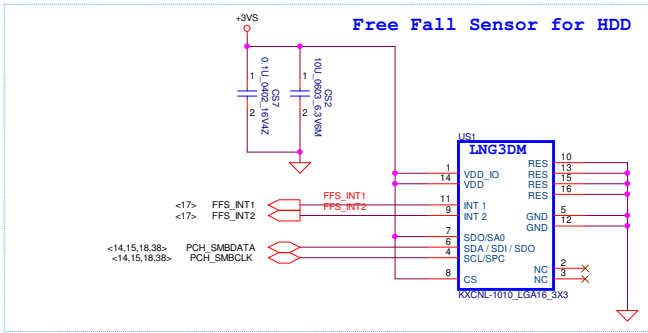


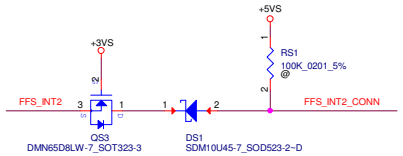
Delete QS2 @01/04, QS1 @01/28



CS8~CS15(0.01U) change to RS9~RS16(0ohm) @01/11







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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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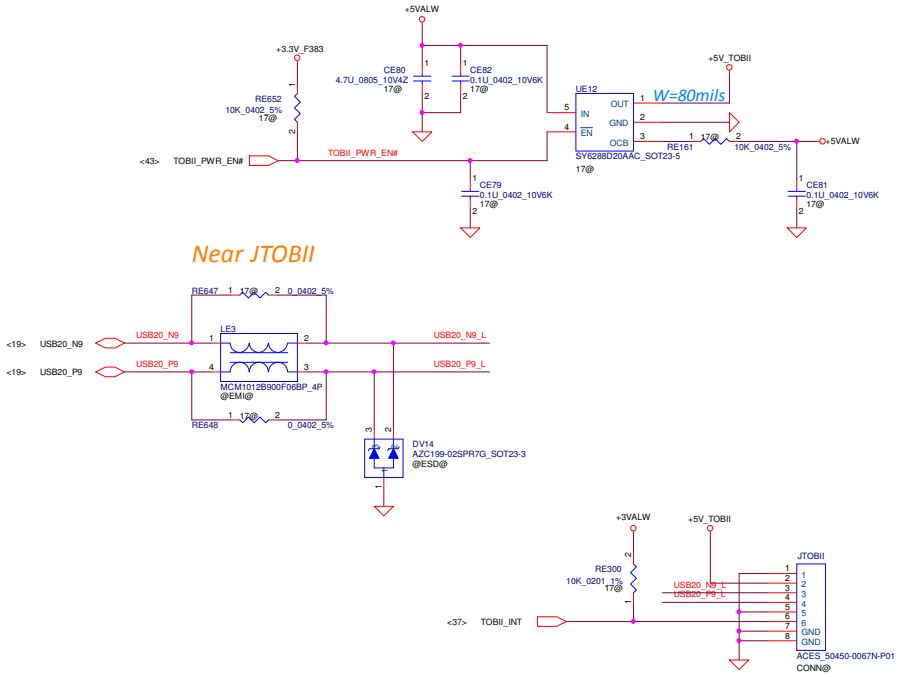
Compal Electronics, Inc.

Title: **SATA HDD Connector**

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 Sheet 33 of 82

Tobii Conn.



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **Tobii (17" Only)**

Size	Document Number	Rev
	LA-D751P	1.0

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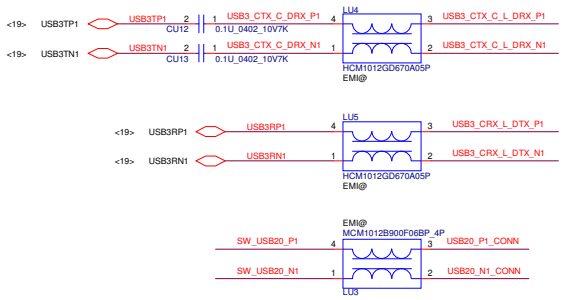
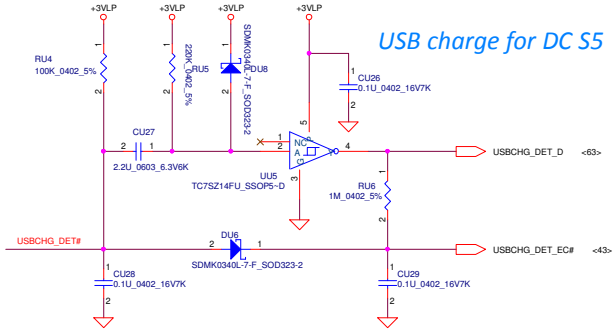
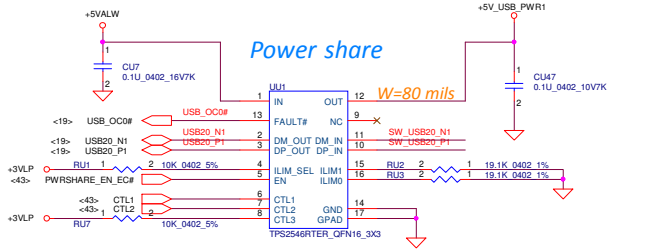
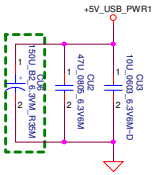
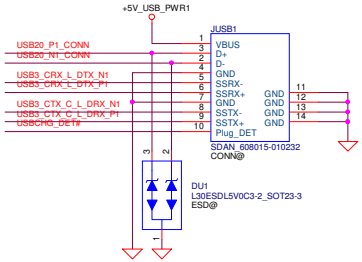
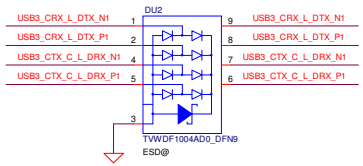


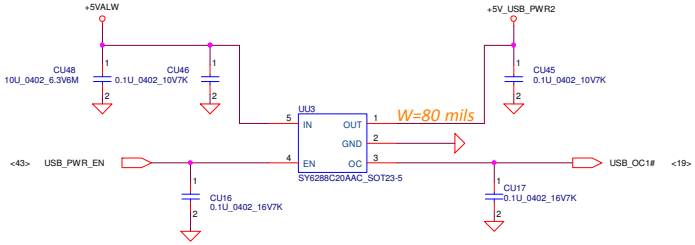




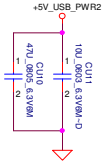




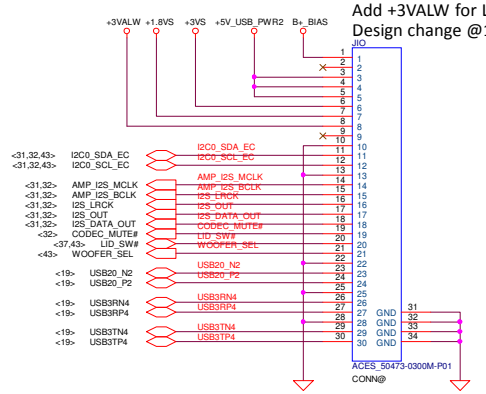




Delete CU43 @12/29



Add +3VALW for Lid @01/08
Design change @12/30



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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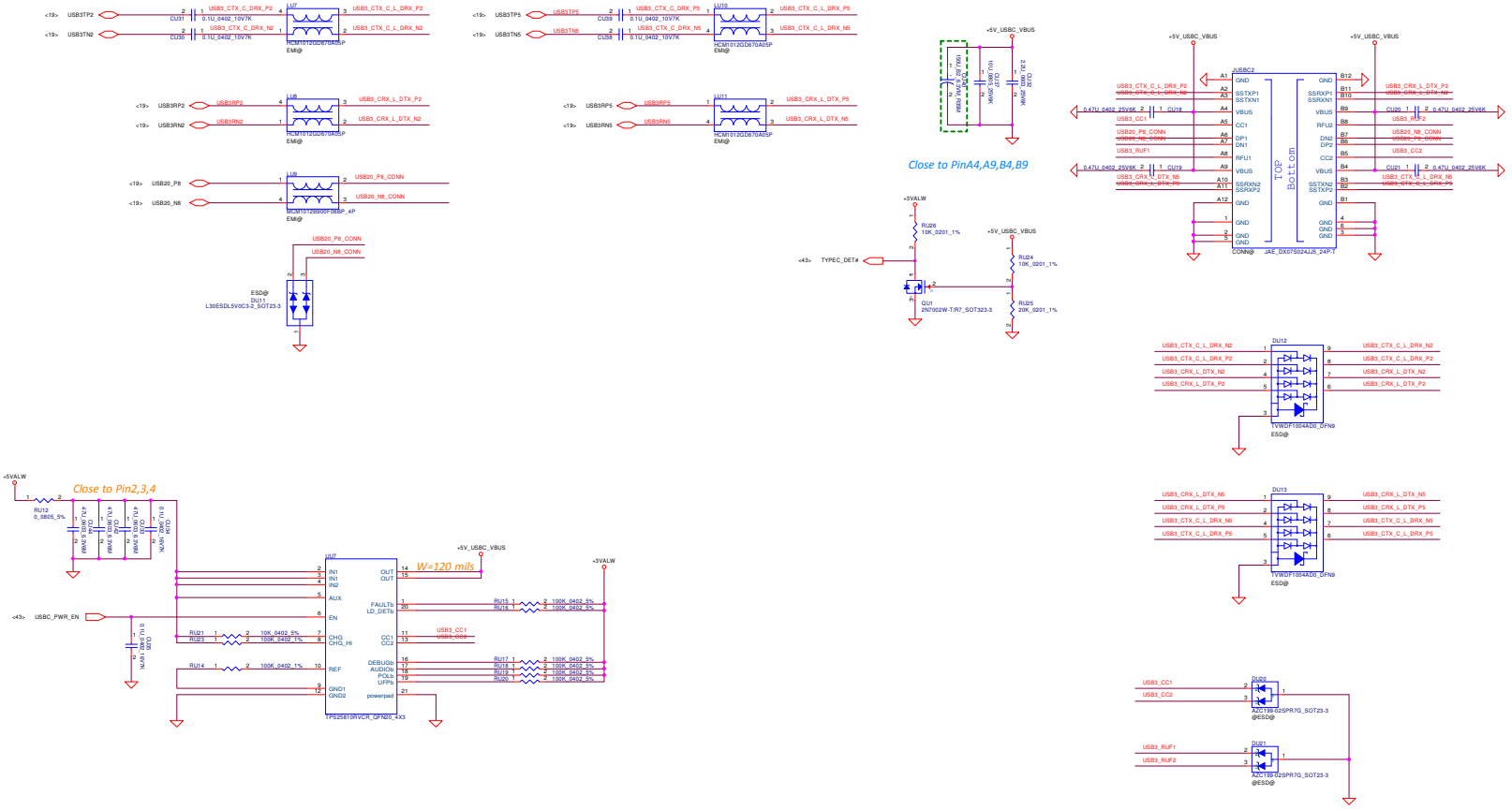
Compal Electronics, Inc.	
Title	USB3.0/2.0 (TypeA+IO/B)
Size	Document Number: LA-D751P
Rev	1.0
Date:	Friday, September 02, 2016
Sheet	35 of 82



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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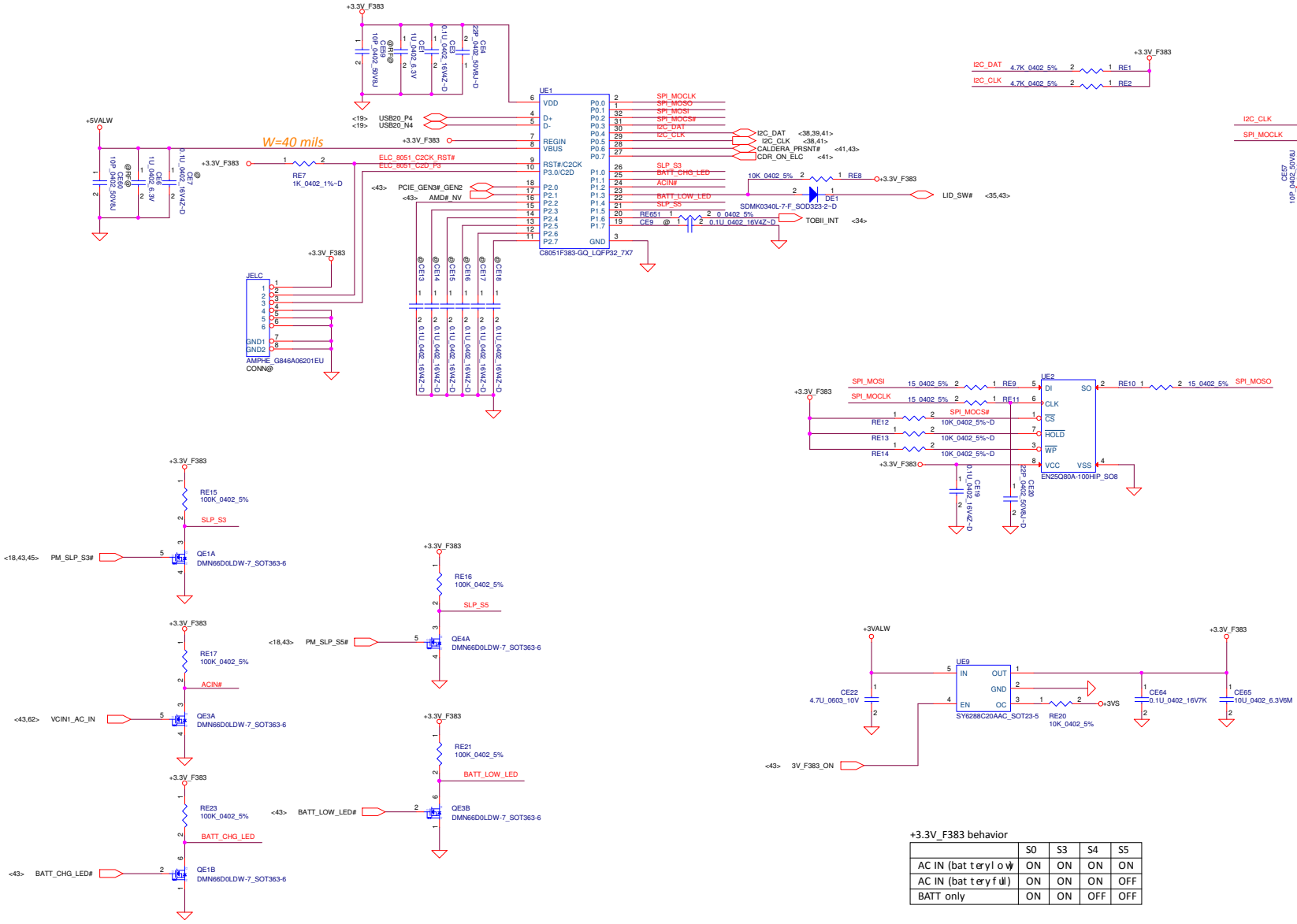
Compal Electronics, Inc.			
Title	USB3.0/2.0 (TypeC)		
Size	Document Number		Rev
	LA-D751P		1.0
Date: Friday, September 02, 2016	Sheet 36 of 82		



+3.3V_F383 behavior

	S0	S3	S4	S5
AC IN (bat teryl ow)	ON	ON	ON	ON
AC IN (bat tery full)	ON	ON	ON	OFF
BATT only	ON	ON	OFF	OFF

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: ELC (1) C8051F383

Size: LA-D751P | Document Number | Rev 1.0

Date: Tuesday, August 16, 2016 | Sheet 37 of 82

AD0 1
AD1 1
AD2 0
AD3 0

AD0 0
AD1 0
AD2 1
AD3 0

TP LED re-driver

Power LED

Touchpad LED circuit

To logo board

Change connector from 14pin to 16pin @12/16

W=20 mils

To power board

To Tron Light board X2

Change connector from 6pin*4 to 12pin*2 @12/16

W=20 mils

To touchpad module

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

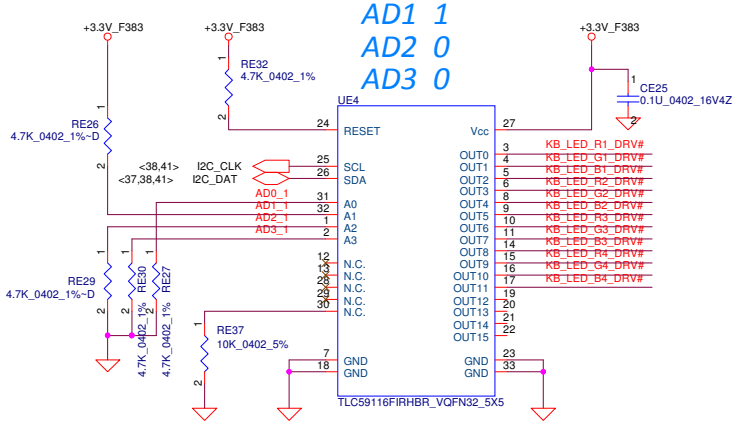
Title: ELC (2) TP/PW/LOGO/TRON

Size: | Document Number: LA-D751P | Rev: 1.0

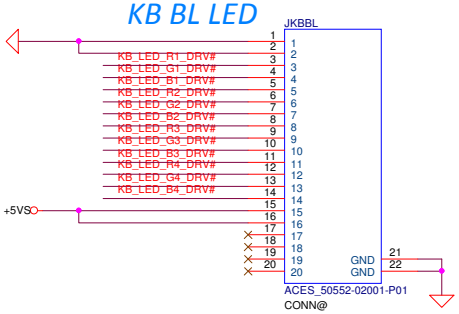
Date: Tuesday, August 16, 2016 | Sheet 38 of 82

KB Backlight

AD0 0
AD1 1
AD2 0
AD3 0



KB BL LED



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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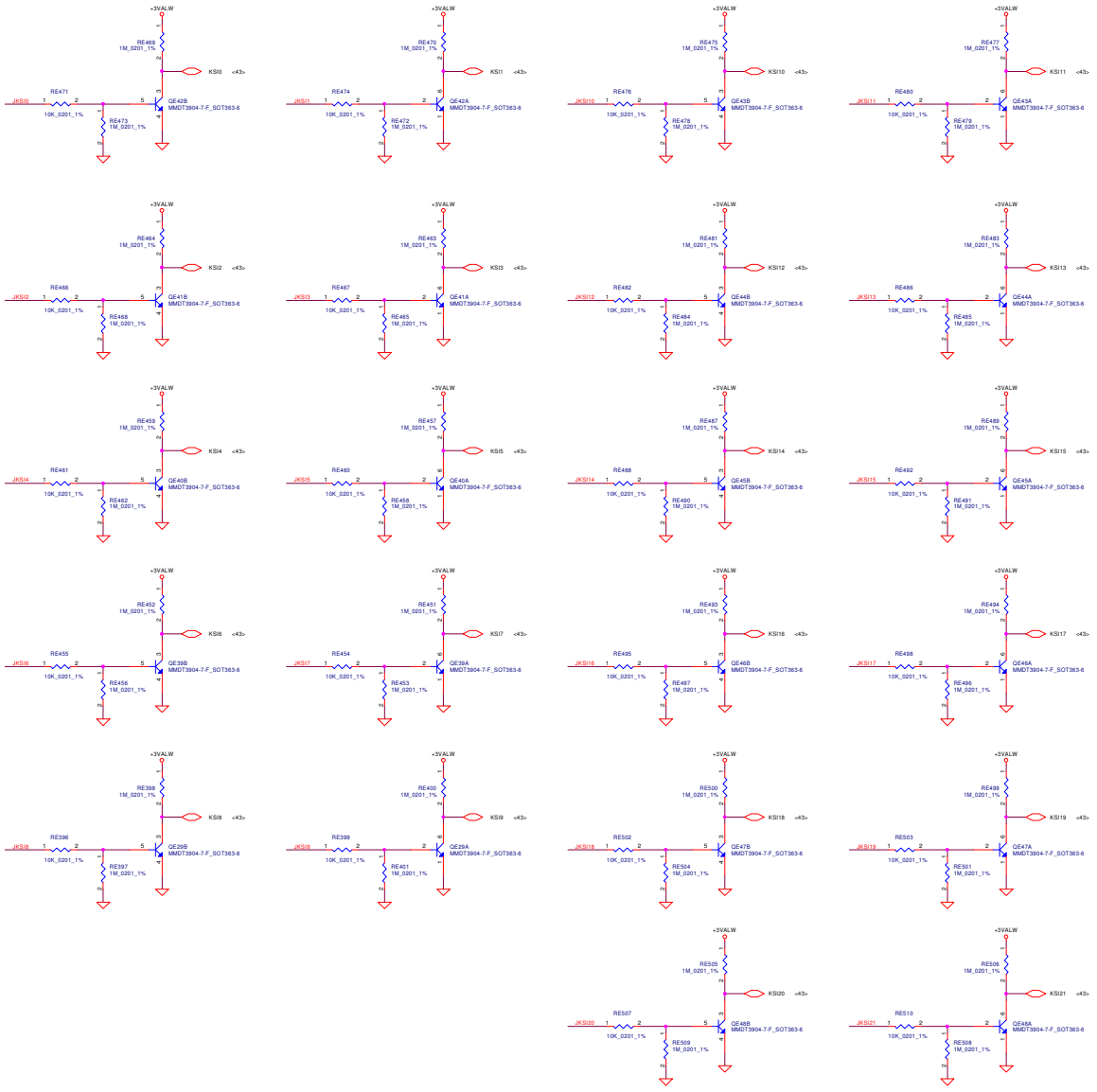
Compal Electronics, Inc.

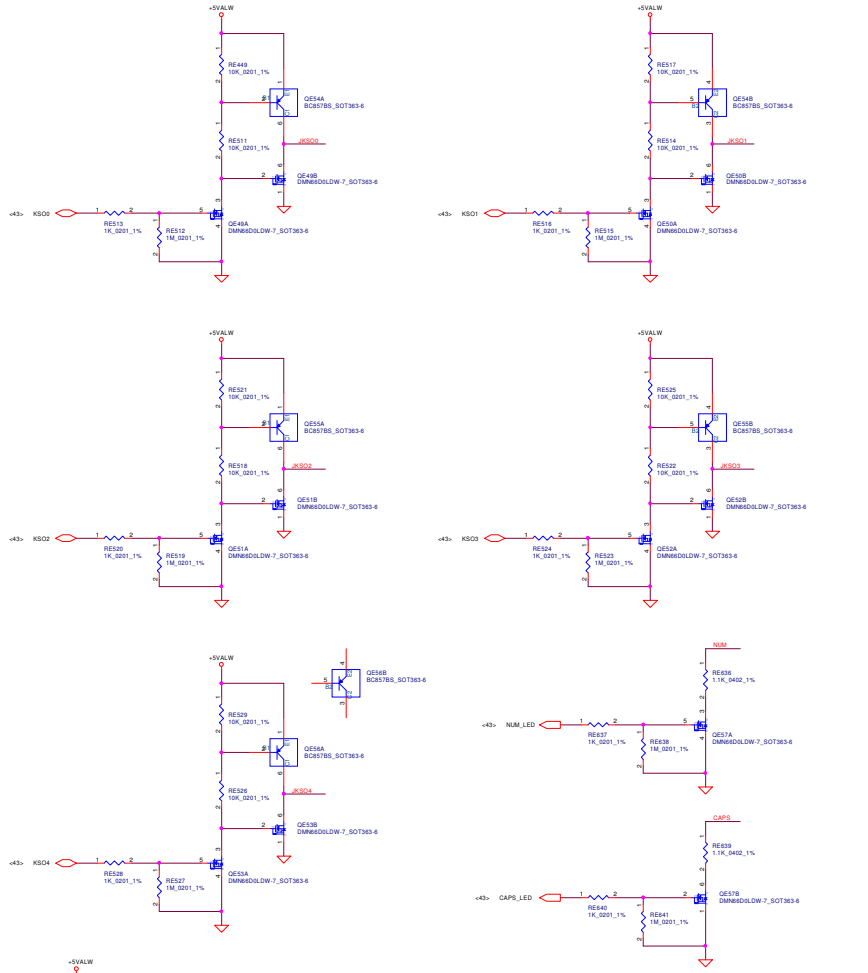
Title: **ELC (3) KBBL**

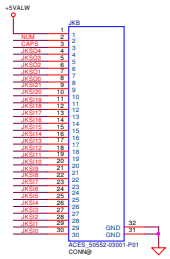
Size | Document Number: **LA-D751P** | Rev: 1.0

Date: Tuesday, August 16, 2016 | Sheet 39 of 82

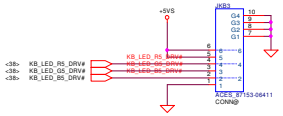
QE54,QE55,QE56 change to SB000018700



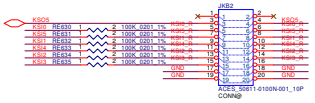




Hot Key Conn. PWM



Hot Key Conn. Key Pad



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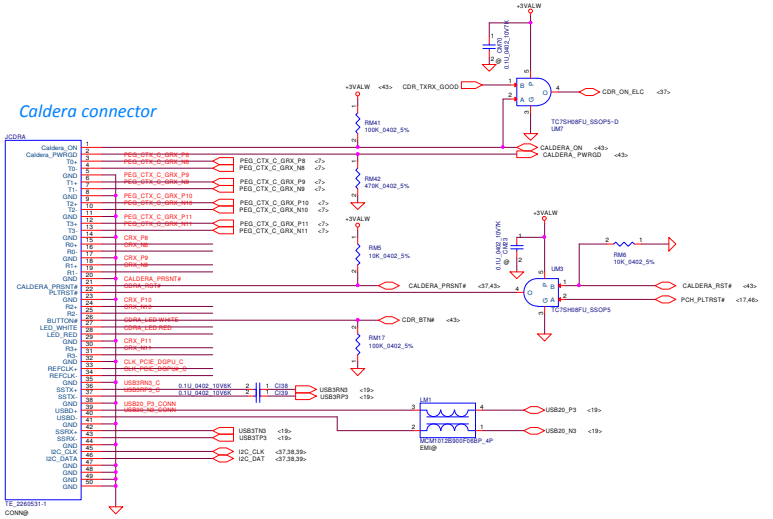
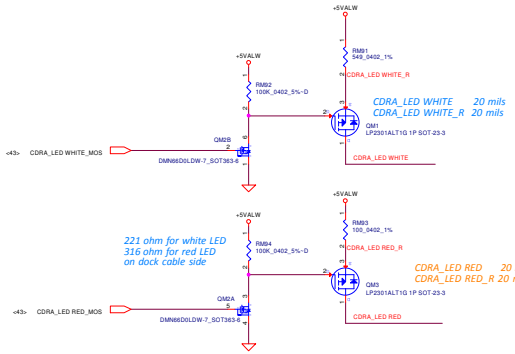
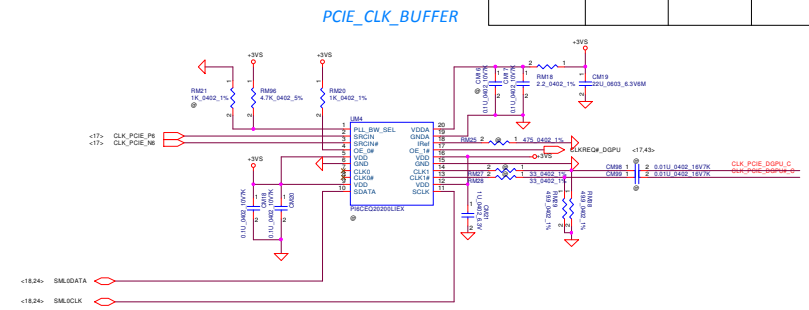
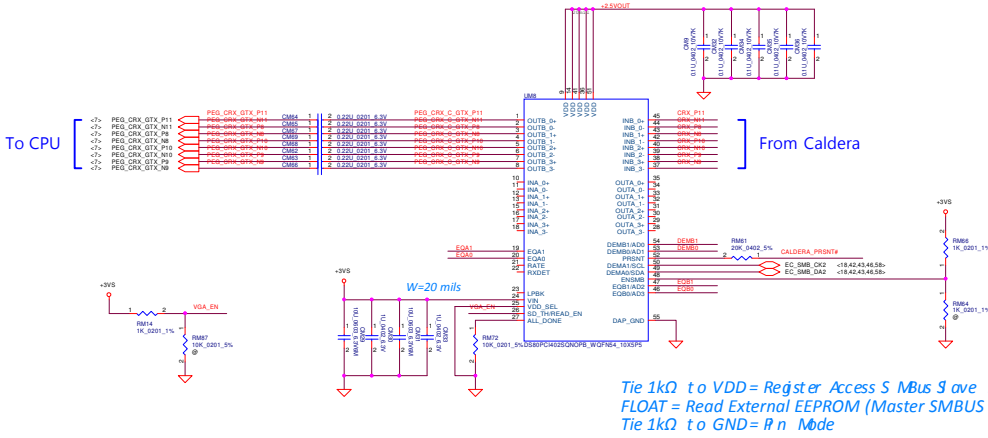
Title	ELC (4) NKRO KB		
Size	Document Number		Rev
	LA-D751P		1.0
Date: Tuesday, August 16, 2016	Sheet 40 of 52		



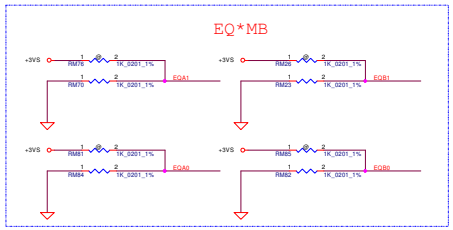


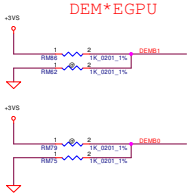
PCIe Clock Buffer	RM25	RM27 / RM28	CM16	CM98 / CM99
★ Pericom (SA00007JZ00) X7669431L7S	SD034475080 (475 +-1% 0402)	SD034330A80 (33 +-1% 0402)	SE102104K00 (0.1U +-10% 0402)	SE076103K80 (.01U 16V K X7R 0402)
IDT (SA00007ZU00) X7669431L7S	SD034412080 (412 +-1% 0402)	SD00000AD80 (27 +-1% 0402)	SE000000LL10 (1U +-10% 0402)	SE076104K80 (.1U 16V K X7R 0402)





Tie 1kΩ to VDD = Register Access SMBus Slave mode
FLOAT = Read External EEPROM (Master SMBUS Mode)
Tie 1kΩ to GND = Pin Mode





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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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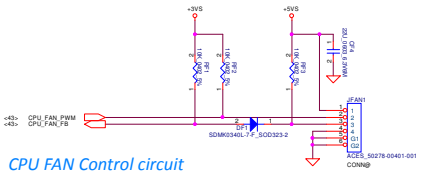
Compal Electronics, Inc.

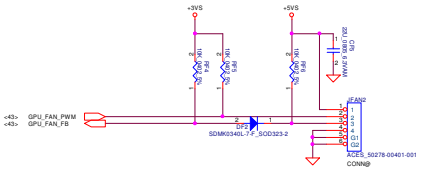
Title: Caldera Docking

Size: | Document Number: LA-D751P | Rev: 1.0

Date: Wednesday, August 24, 2016 | Sheet 41 of 52

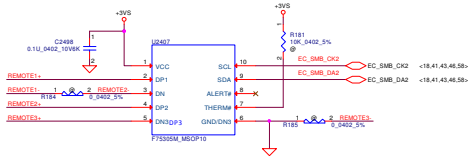


CPU FAN Control circuit



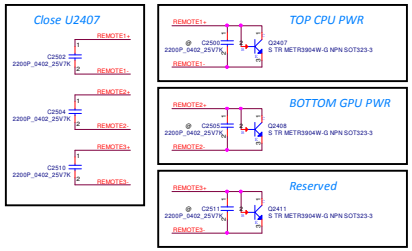
GPU FAN Control circuit

Fintek thermal sensor---> CPU core, DIMM



Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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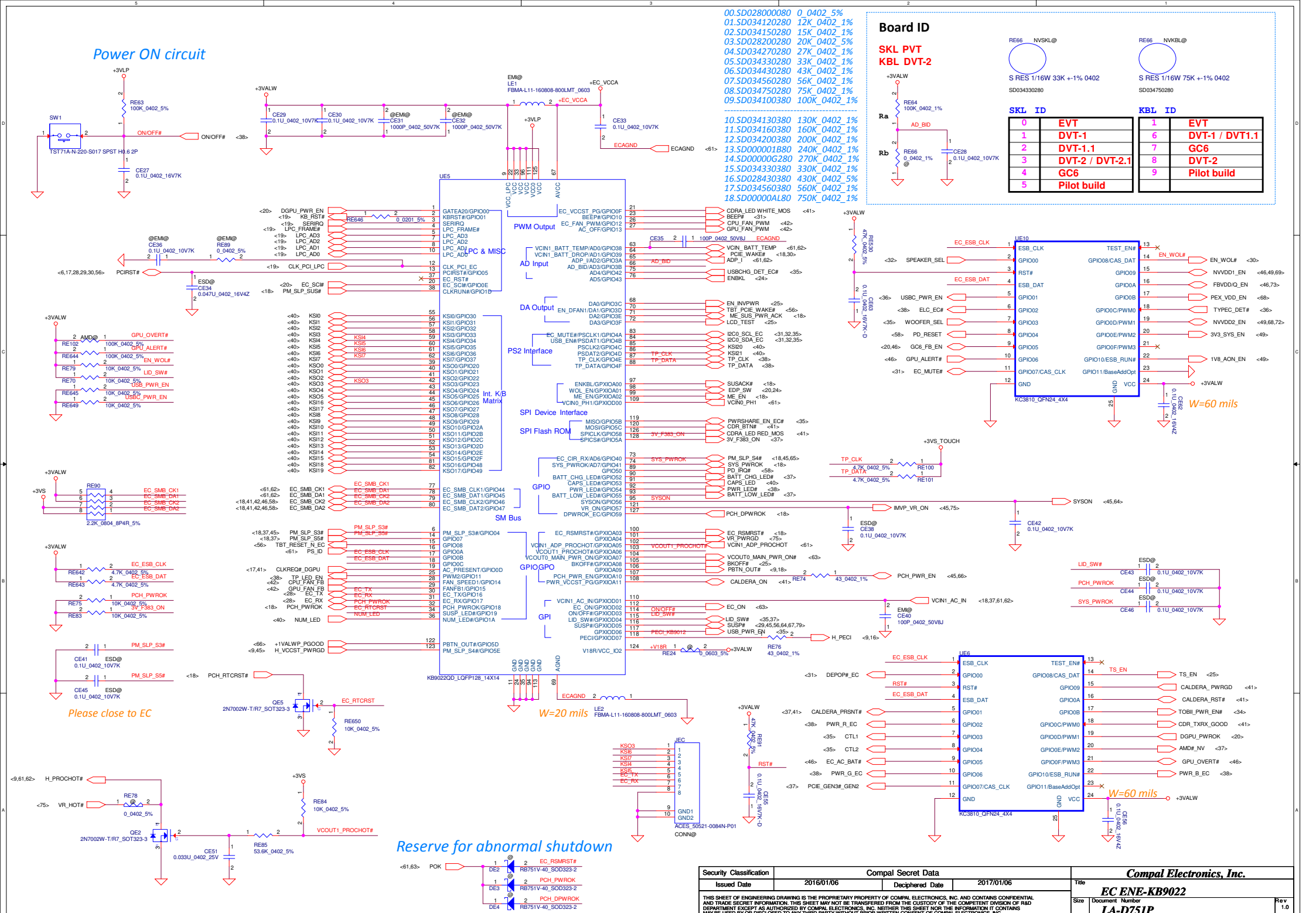
Compal Electronics, Inc.			
Title: FAN/Thermal			
Size	Document Number: LA-D751P		Rev: 1.0
Date: Tuesday, August 16, 2016	Sheet 42 of 82		



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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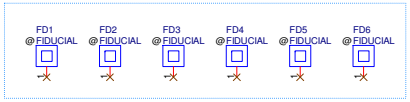
Compal Electronics, Inc.

Title: EC ENE-KB9022

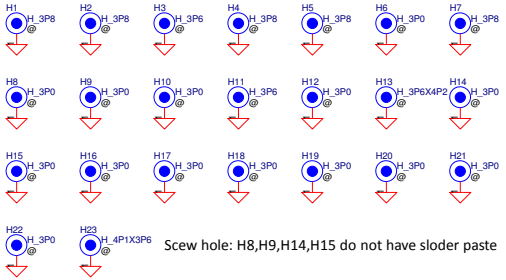
Size: | Document Number: LA-D751P | Rev: 1.0

Date: Tuesday, August 23, 2016 | Sheet 43 of 82

Fiducial Mark



PCB Screw Hole



Scew hole: H8,H9,H14,H15 do not have sloder paste

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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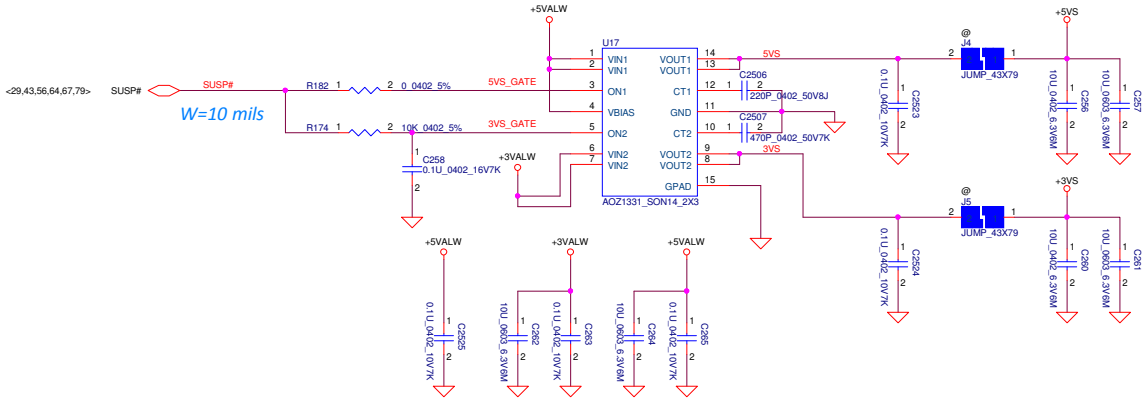
Compal Electronics, Inc.

Title: **Screw Hole**

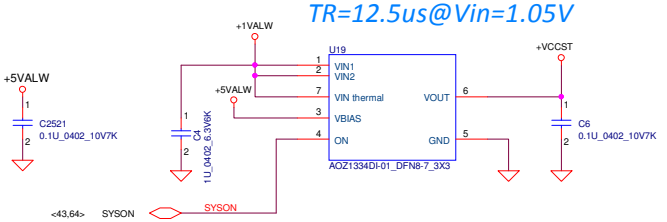
Size | Document Number: **LA-D751P** | Rev: 1.0

Date: Tuesday, August 16, 2016 | Sheet 44 of 82

+5VS and +3VS switch
20mohm/6A per channel

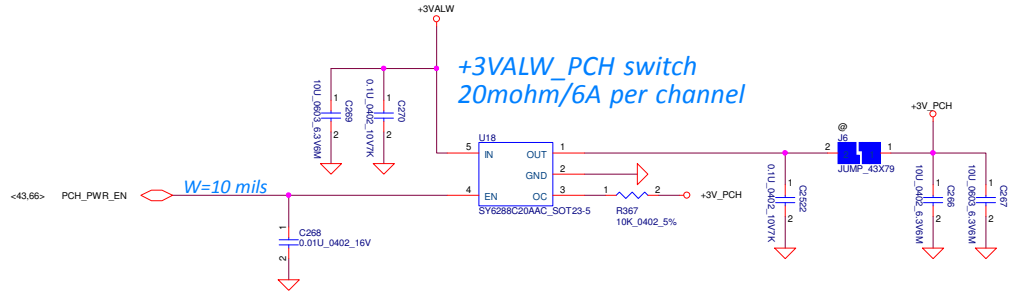


+VCCST switch
4.4mohm/6A
TR=12.5us@Vin=1.05V

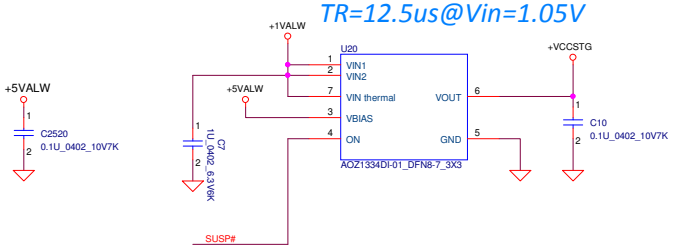


Main source AOS SA00008A800 (SIC AOZ1334DI-01 DFN8P SINGLE LOADSW)
2nd source APEC SA00006V300 (SIC APE8939GN3 DFN8P LOADSWITCH)
3rd source EMC SA00008R600 (SIC EM5201V DFN3X3 8P LOADSWITCH)

+3VALW_PCH switch
20mohm/6A per channel



+VCCSTG switch
4.4mohm/6A
TR=12.5us@Vin=1.05V

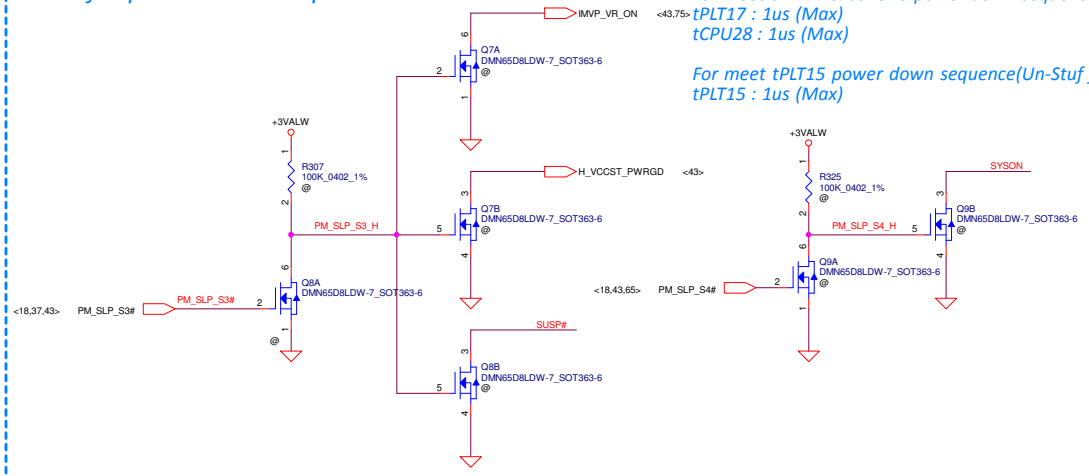


Main source AOS SA00008A800 (SIC AOZ1334DI-01 DFN8P SINGLE LOADSW)
2nd source APEC SA00006V300 (SIC APE8939GN3 DFN8P LOADSWITCH)
3rd source EMC SA00008R600 (SIC EM5201V DFN3X3 8P LOADSWITCH)

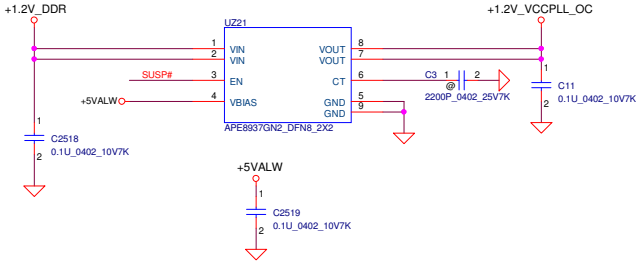
add for power down sequence

For meet tPLT17 & tCPU28 power down sequence.
tPLT17 : 1us (Max)
tCPU28 : 1us (Max)

For meet tPLT15 power down sequence(Un-Stuf f)
tPLT15 : 1us (Max)



+1.2V_VCCPLL_OC switch
22mohm/4A
TR=520us@Vin=0.8V



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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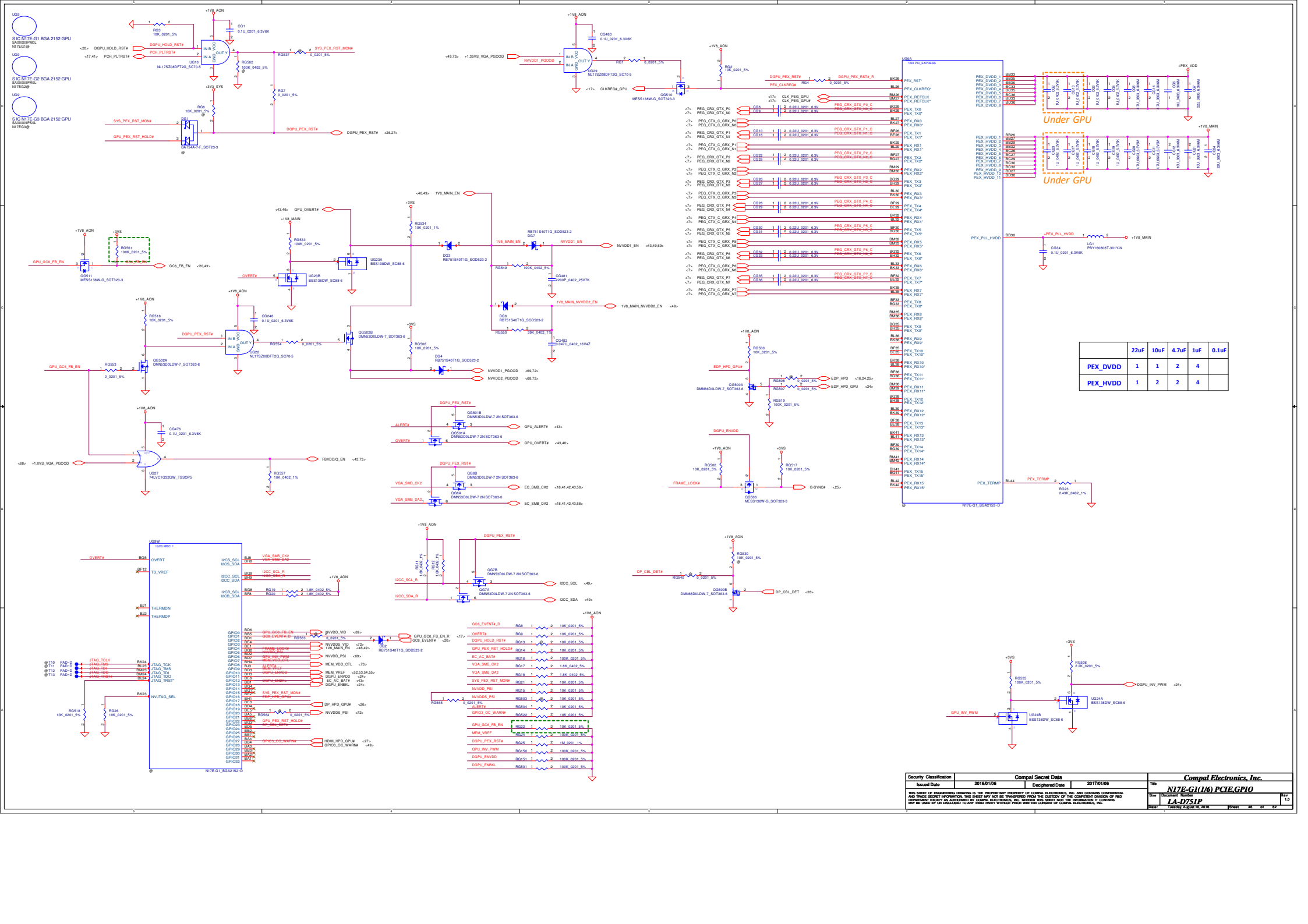
Compal Electronics, Inc.

Title: **DC/DC Interface**

Size | Document Number: **LA-D751P** | Rev: 1.0

Date: Tuesday, August 16, 2016 | Sheet 45 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
PEX_DVDD	1	1	2	4	
PEX_HVDD	1	2	2	4	

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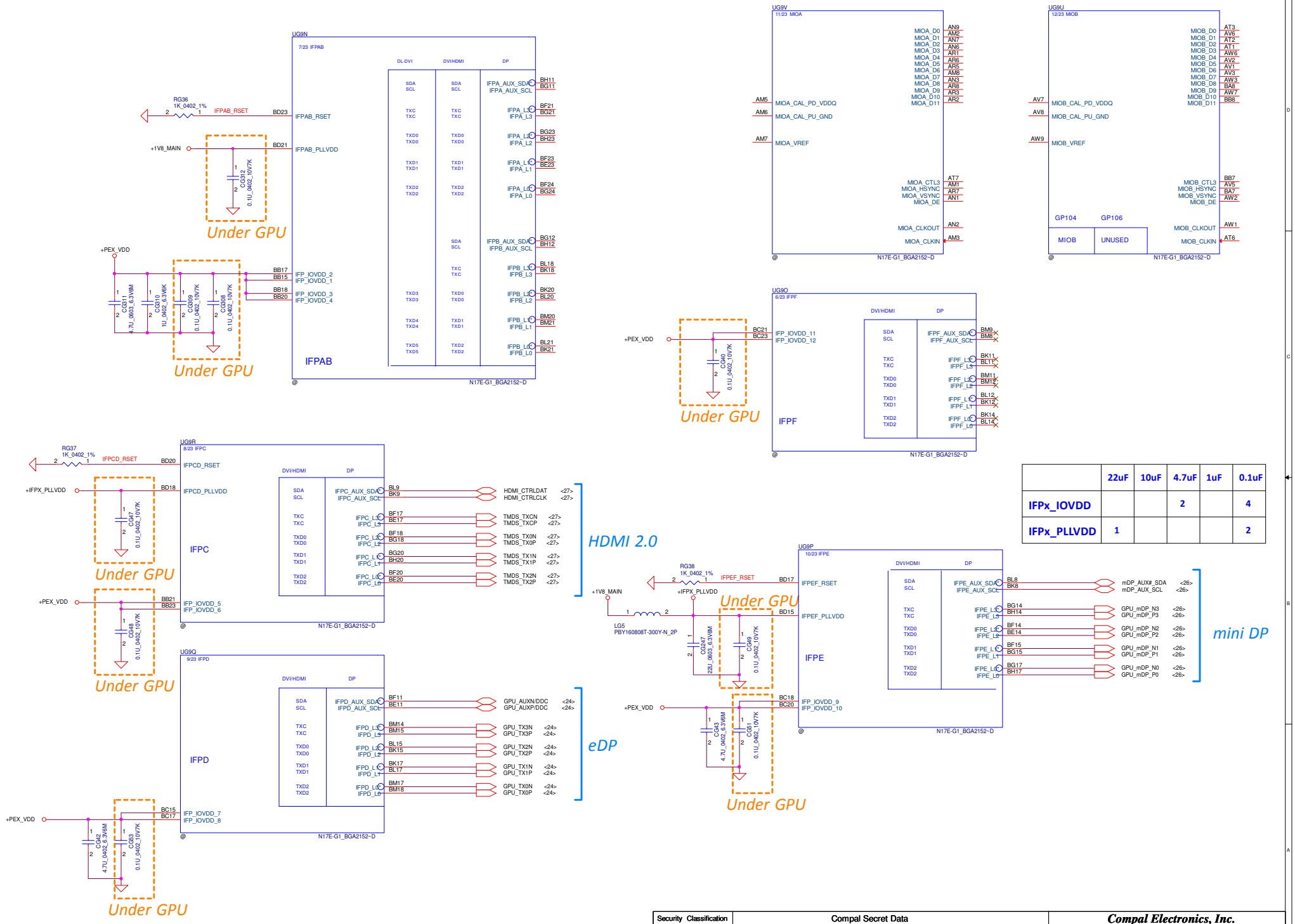

	22uF	10uF	4.7uF	1uF	0.1uF
IFPx_IOVDD			2		4
IFPx_PLLVDD	1				2

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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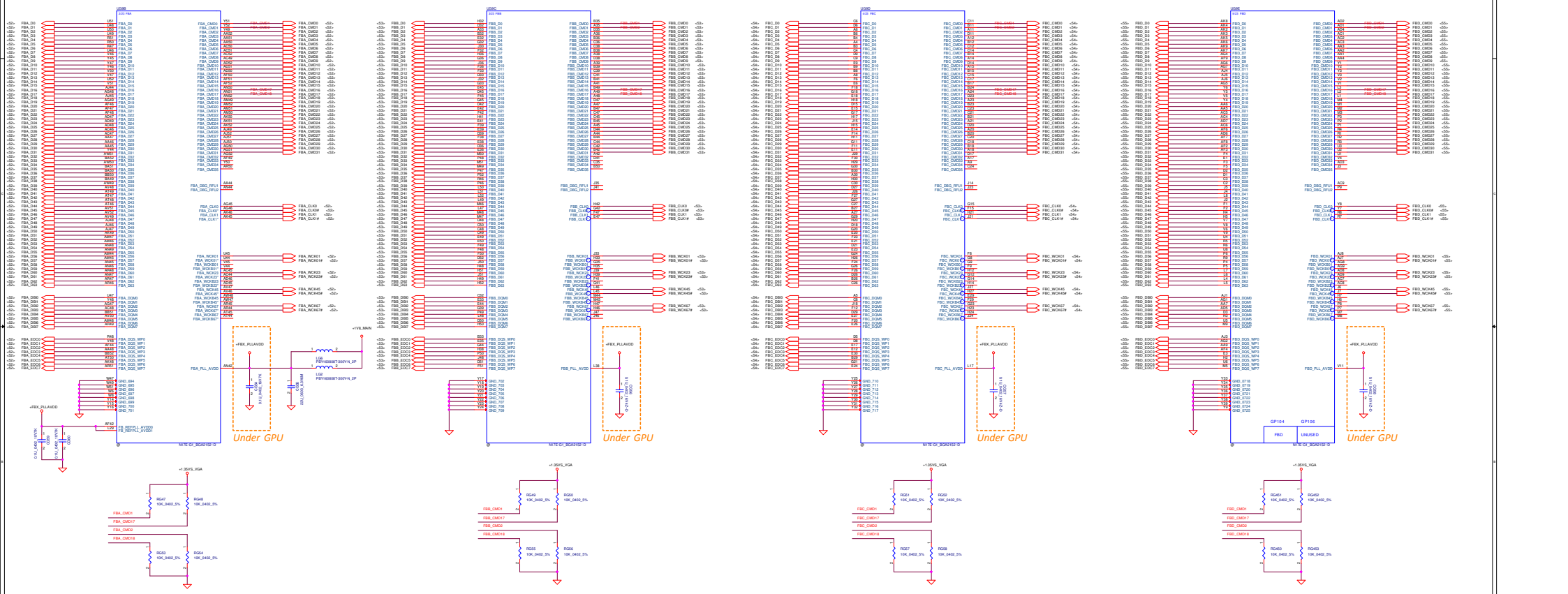
Compal Electronics, Inc.

Title: N17E-G1(2/6) eDP,HDMI,mDP

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 | Sheet 47 of 82



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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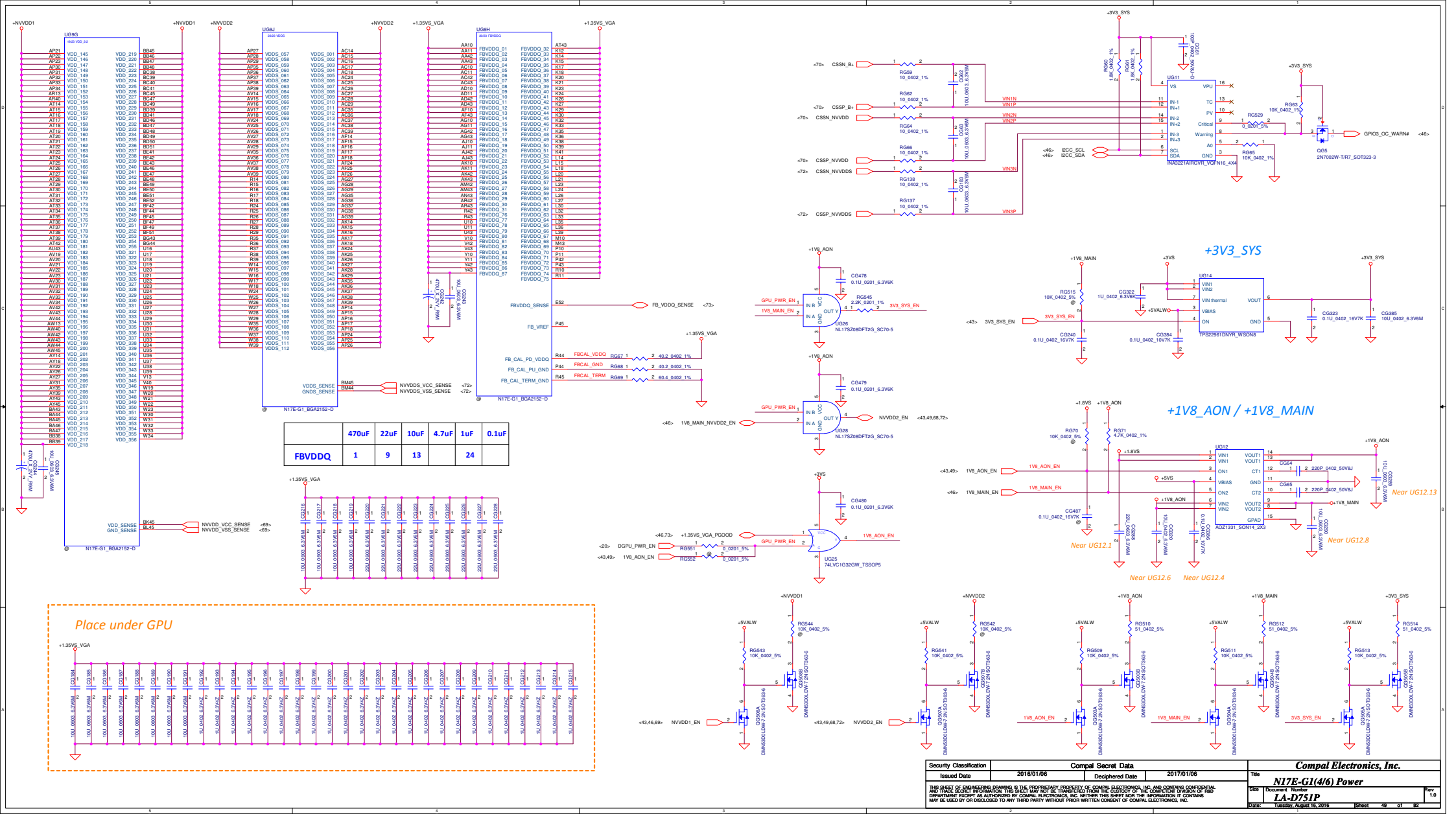
Compal Electronics, Inc.			
Title: N17E-G1(3/6) MEM Interface			
Size:	Document Number: LA-D751P		Rev: 1.0
Date: Tuesday, August 15, 2016	Sheet: 46	of: 60	



	470uF	22uF	10uF	4.7uF	1uF	0.1uF
FBVDDQ	1	9	13		24	

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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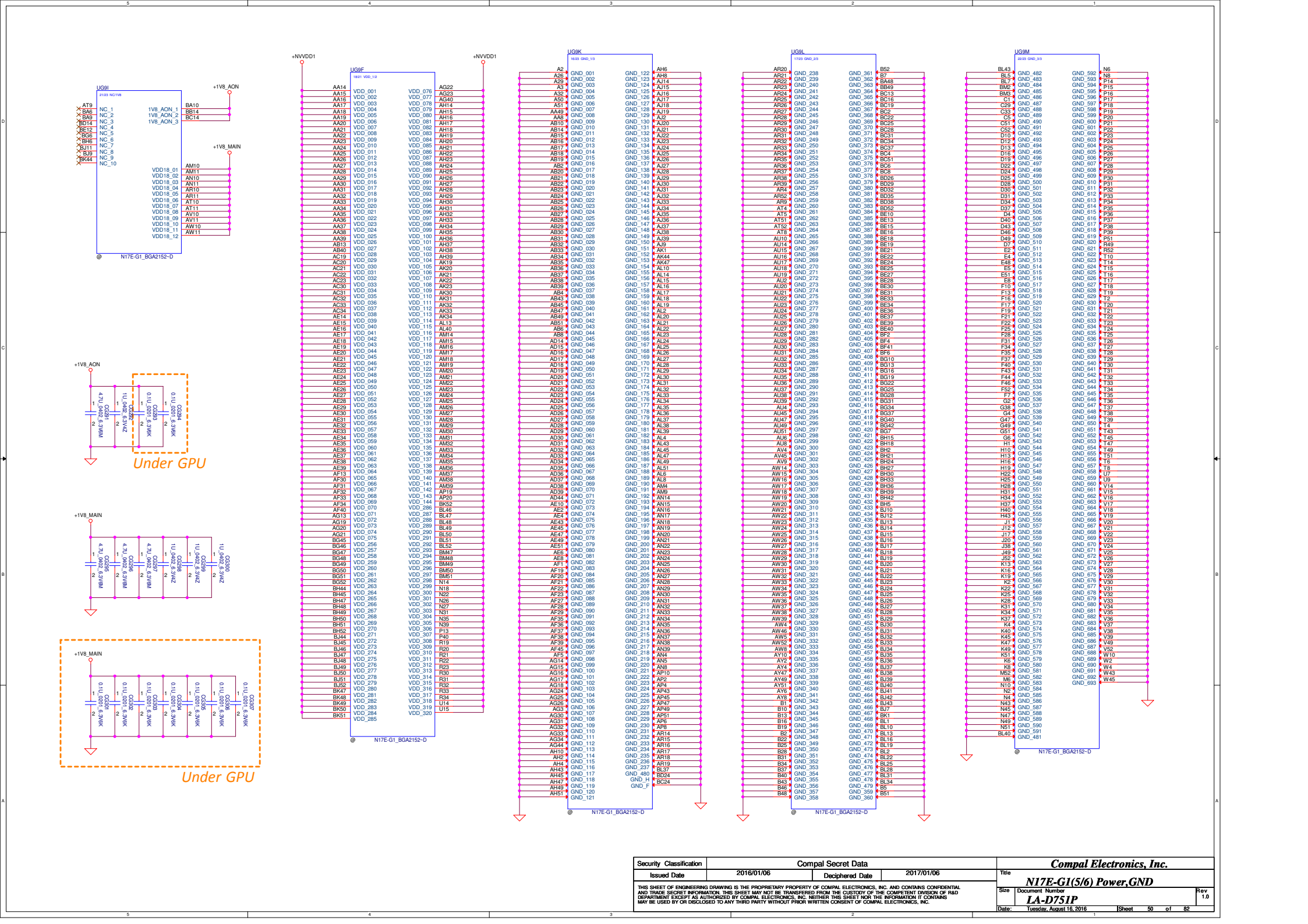
Compal Electronics, Inc.	
Title	N17E-G1(4/6) Power
Size	Document Number: LA-D751P
Rev	1.0
Date:	Tuesday, August 16, 2016
Sheet	49 of 82



Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **N17E-G1(5/6) Power,GND**

Size	Document Number	Rev
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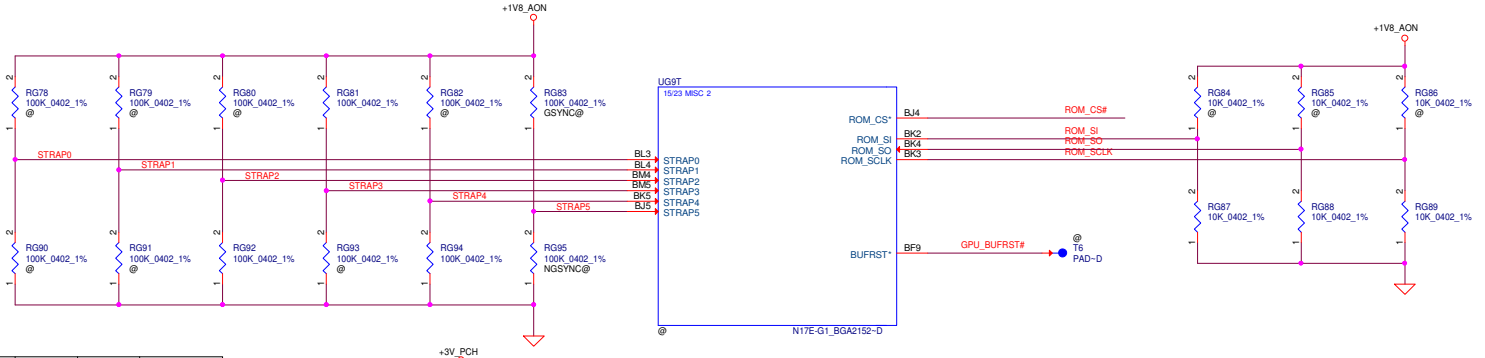
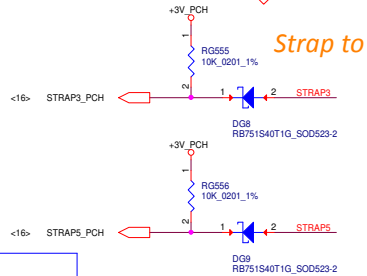
Date: Tuesday, August 16, 2016 | Sheet 50 of 82

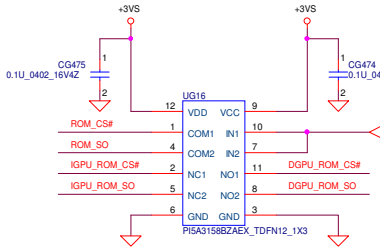
	47uF	22uF	10uF	4.7uF	1uF	0.1uF
VID_PLLVDD	1		1			1
SP_PLLVDD GPCPLL_AVDD		1				6



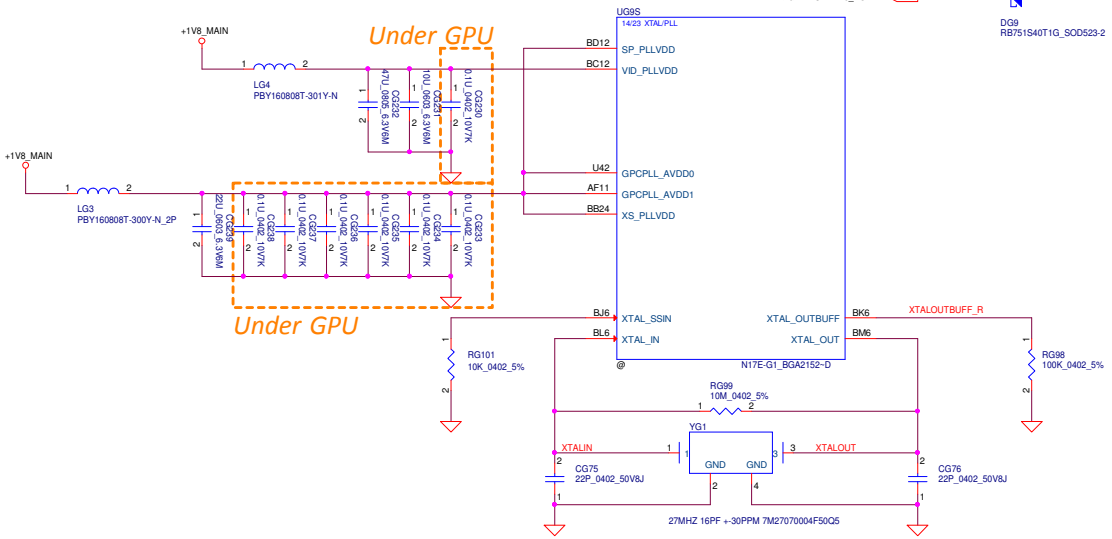
GDDR5 VRAM	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	RAMCFG
SAMSUNG K4G80325FB-HC25 SAMSUNG K4G41325FE-HC28	L	L	L	H	L		0
MICRON MT51J256M32HF-80:A	H	L	L	H	L		1
HYNIX H5GC4H24AJR-R0C	L	H	L	H	L		2

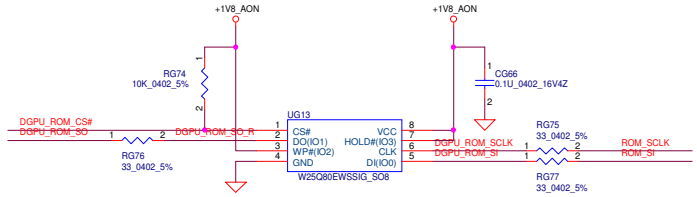
Strap to PCH



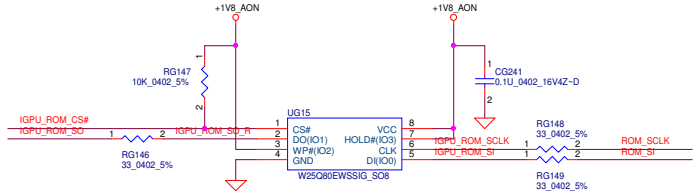


Funct i on	VROM_SEL
COM = NC	L
COM = NO	H





DGPU VBIOS ROM



Optimus VBIOS ROM

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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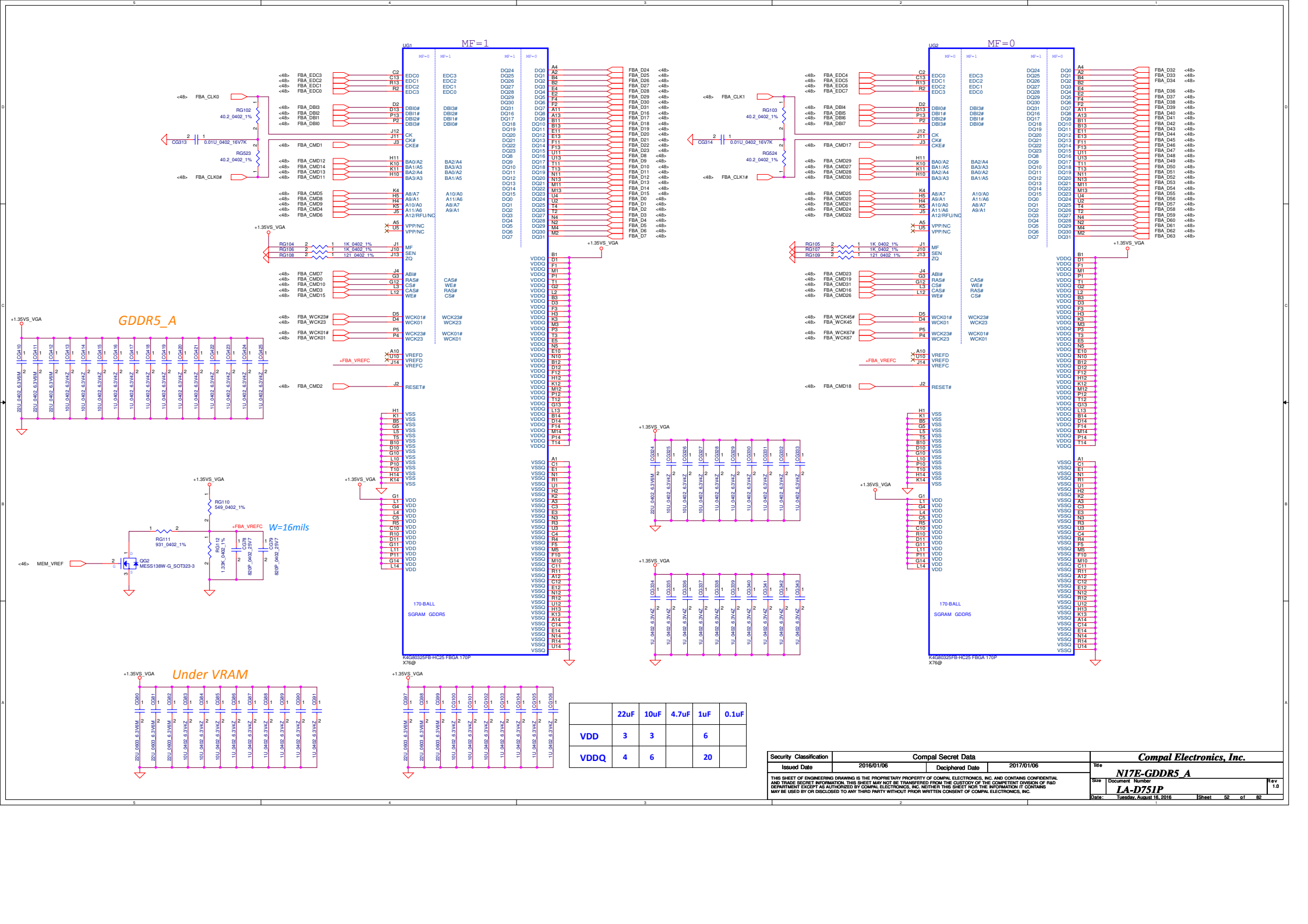
Compal Electronics, Inc.

Title: N17E-G1(6/6) Strap Pin,ROM

Size	Document Number	Rev
	LA-D751P	1.0

Date: Tuesday, August 16, 2016 Sheet 51 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	4	6		20	

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.	
Title	N17E-GDDR5_A
Size	Document Number: LA-D751P
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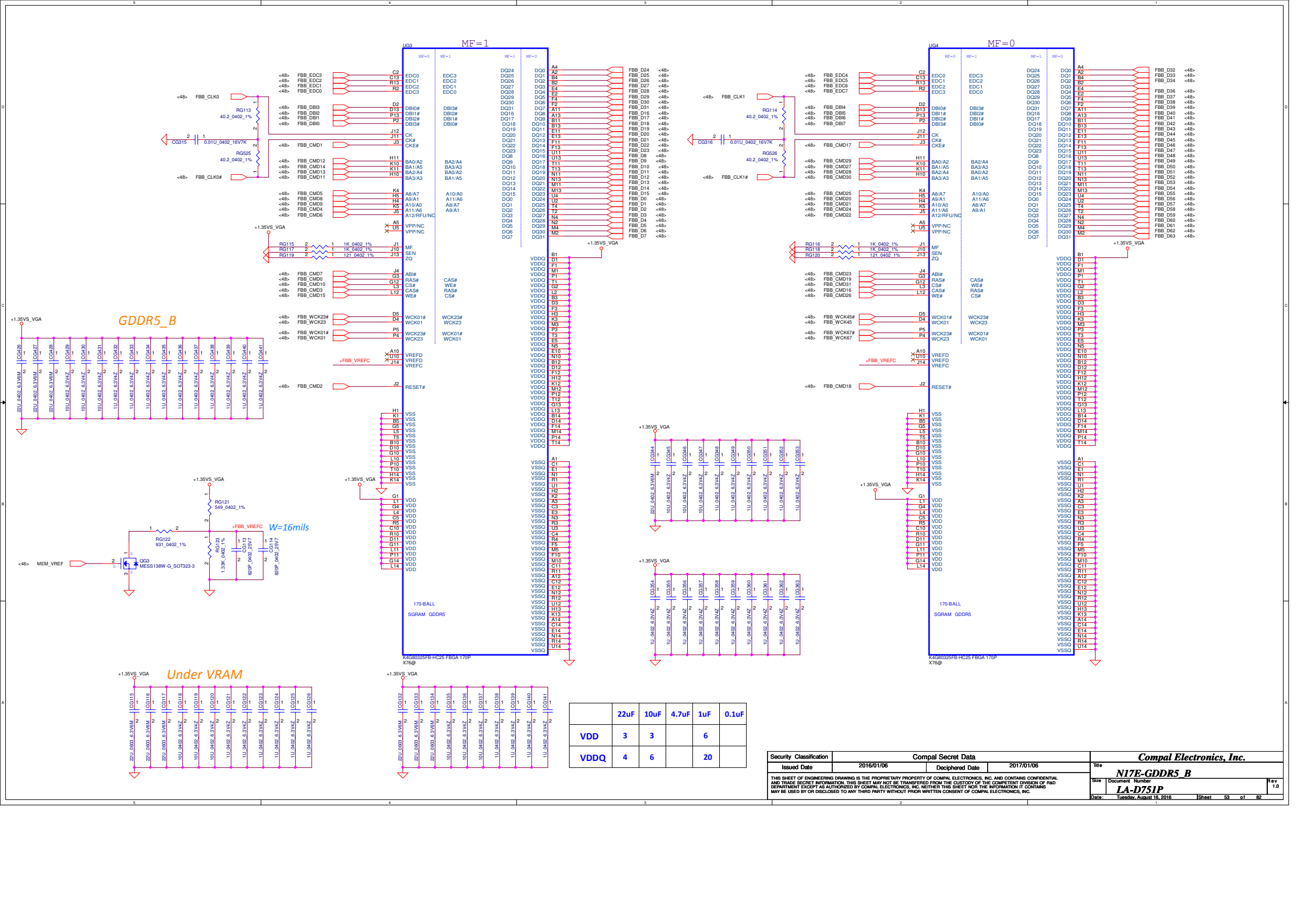
Date:	Tuesday, August 16, 2016
Sheet	52 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	4	6		20	

Security Classification	Compal Secret Data	
Issued Date	2016/01/06	Deciphered Date 2017/01/06

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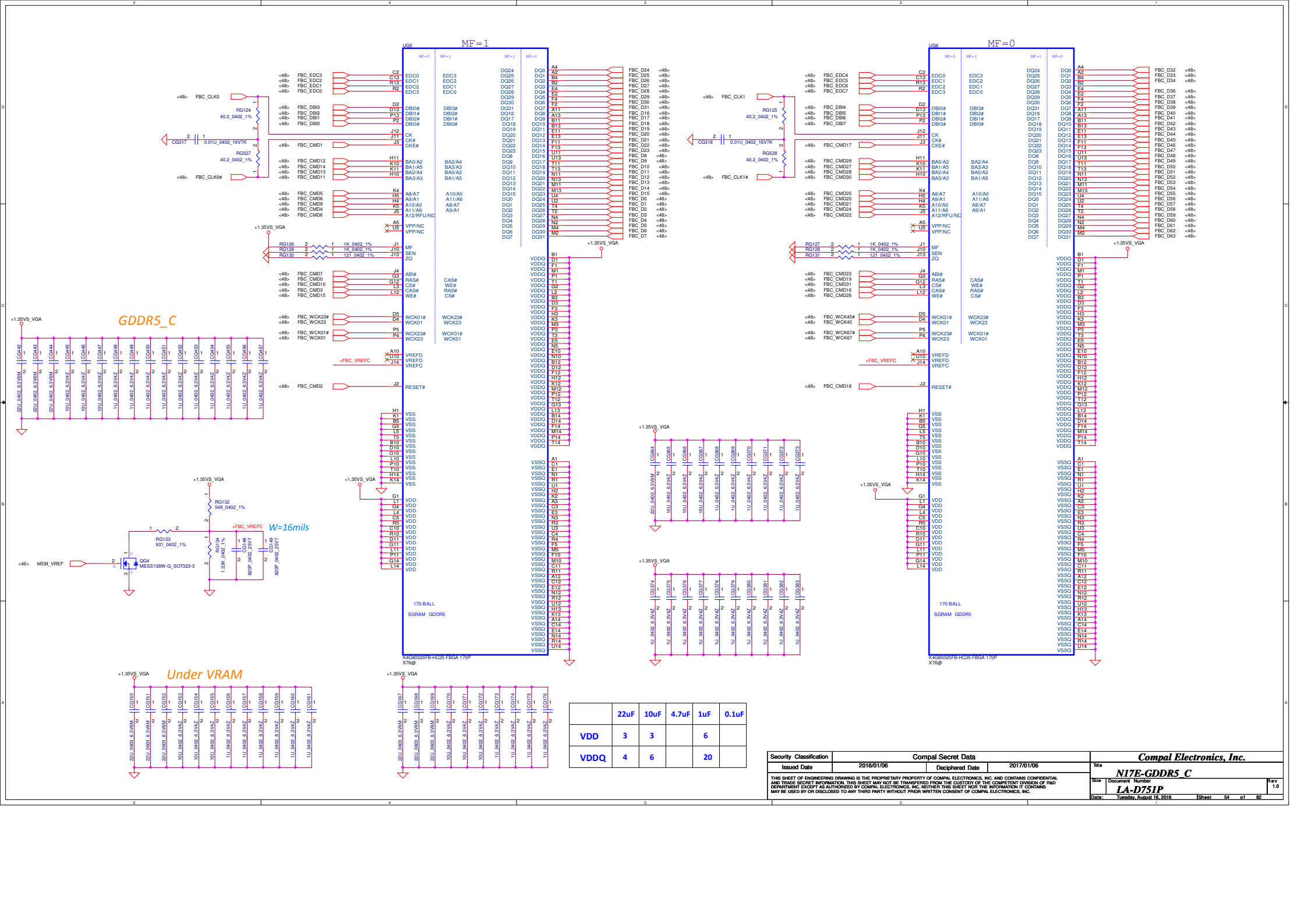
Compal Electronics, Inc.

Title: N17E-GDDR5_B

Size: Document Number: LA-D751P

Rev: 1.0

Date: Tuesday, August 16, 2016 Sheet 53 of 82



	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	4	6		20	

Security Classification	Compal Secret Data	
Issued Date	2016/01/06	Deciphered Date 2017/01/06

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Compal Electronics, Inc.

Title: N17E-GDDR5_C

Size: Document Number: LA-D751P | Rev: 1.0

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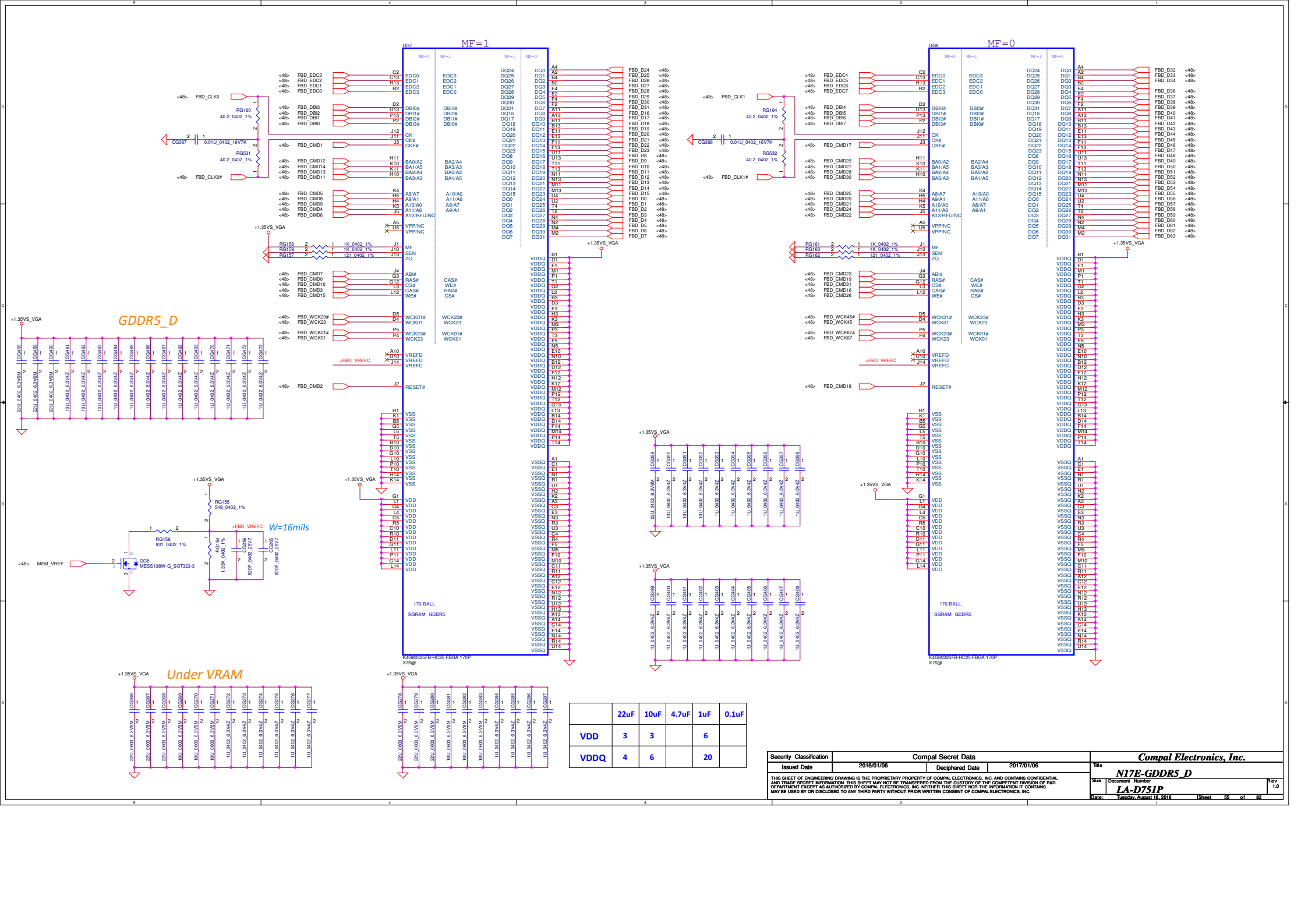

	22uF	10uF	4.7uF	1uF	0.1uF
VDD	3	3		6	
VDDQ	4	6		20	

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: N17E-GDDR5_D

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UT1

S IC A31 JHL6340 QSTZ C0 THUNDERBOLT
SA00009YL0L
ARC0R1@

UT1

S IC JHL6340 SLLSP C1 THUNDERBOLT A31!
SA00009YL3L
ARC1R3@

PEG X4 Bus

PEG_CLK
(From PCH CLKOUT3)

CPU DDI1

Reserve for common DP design

CPU DDI2

UT1A

PCIe GEN3

SINK PORT 0

SOURCE PORT 0

SINK PORT 1

LC GPIO

POC GPIO

Misc

MISC

TBT PORTS

Port A

PORT B

POC

DEBUG

ALPINE-RIDGE_BGA337

Closed to UT1

Close to UT2

Metal Shielding Type

+3.3V_TBT_SX

+3VS_TBT

+3.3V_LC

+3VS

+3.3V_FLASH

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Compal Electronics, Inc.

Title: **Thunderbolt (1/2)**

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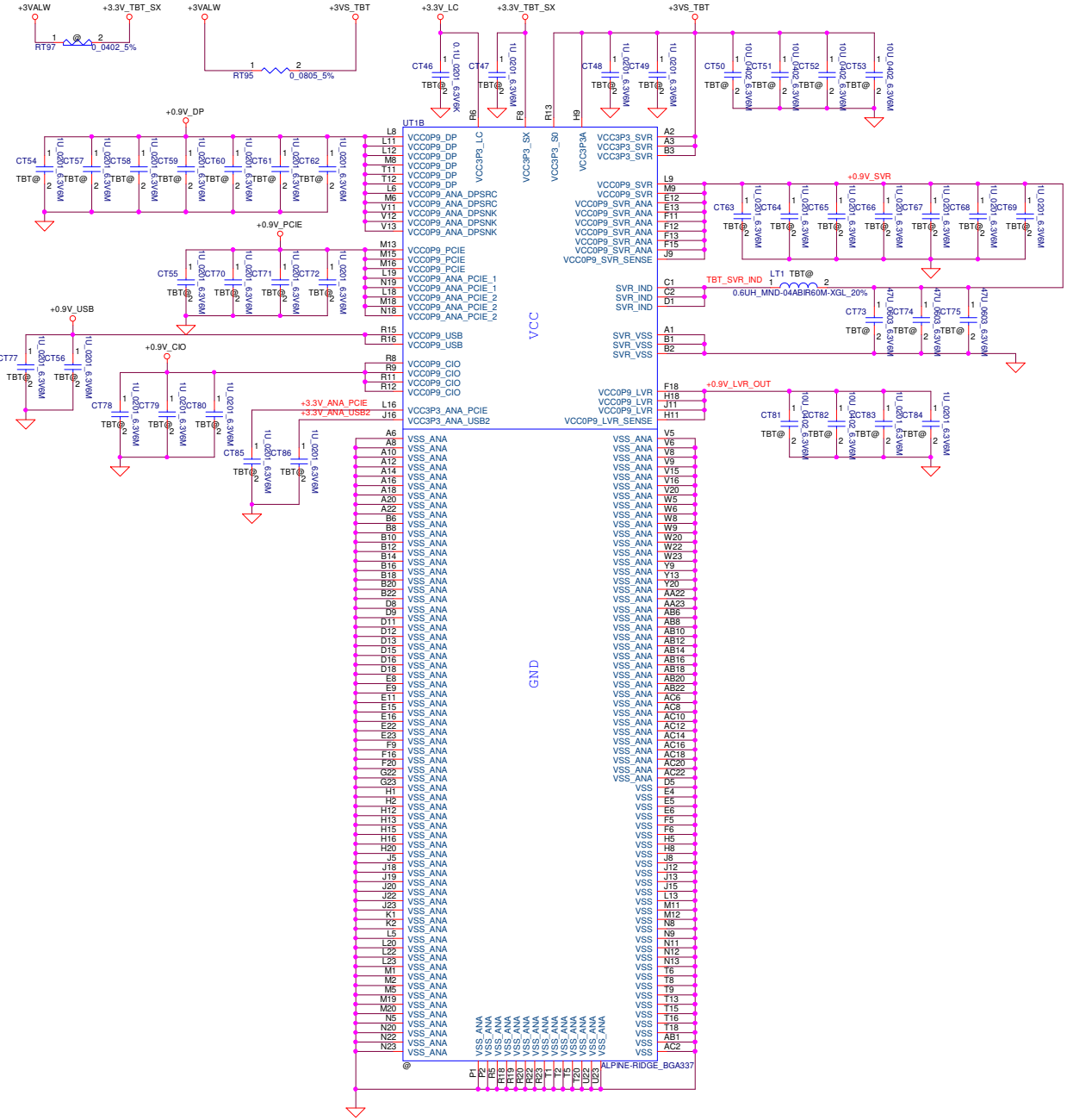
Delete RT104 for layout @12/31

Delete RT52 for layout @12/31



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Compal Electronics, Inc.

Title: Thunderbolt (2/2)

Size	Document Number	Rev
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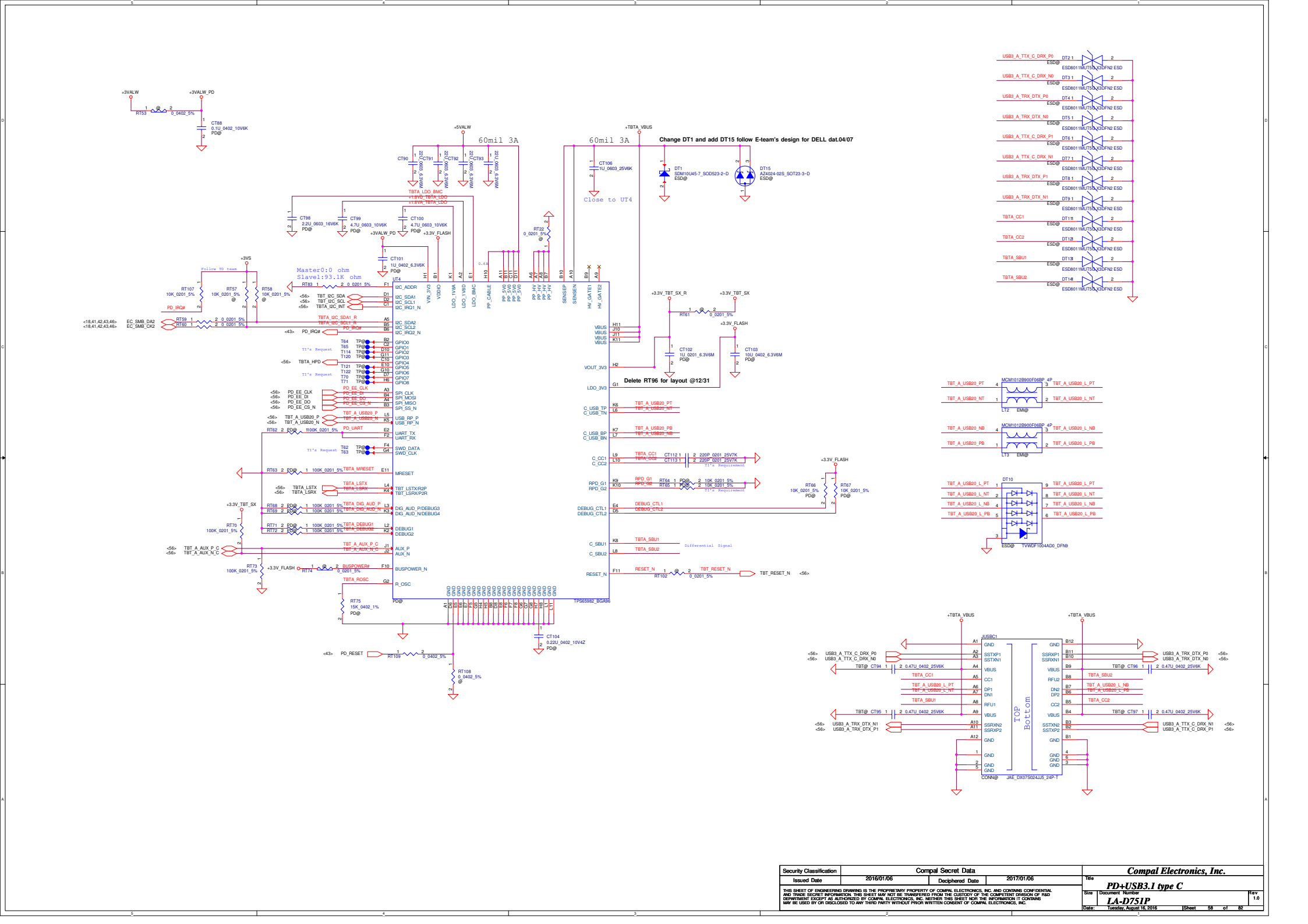
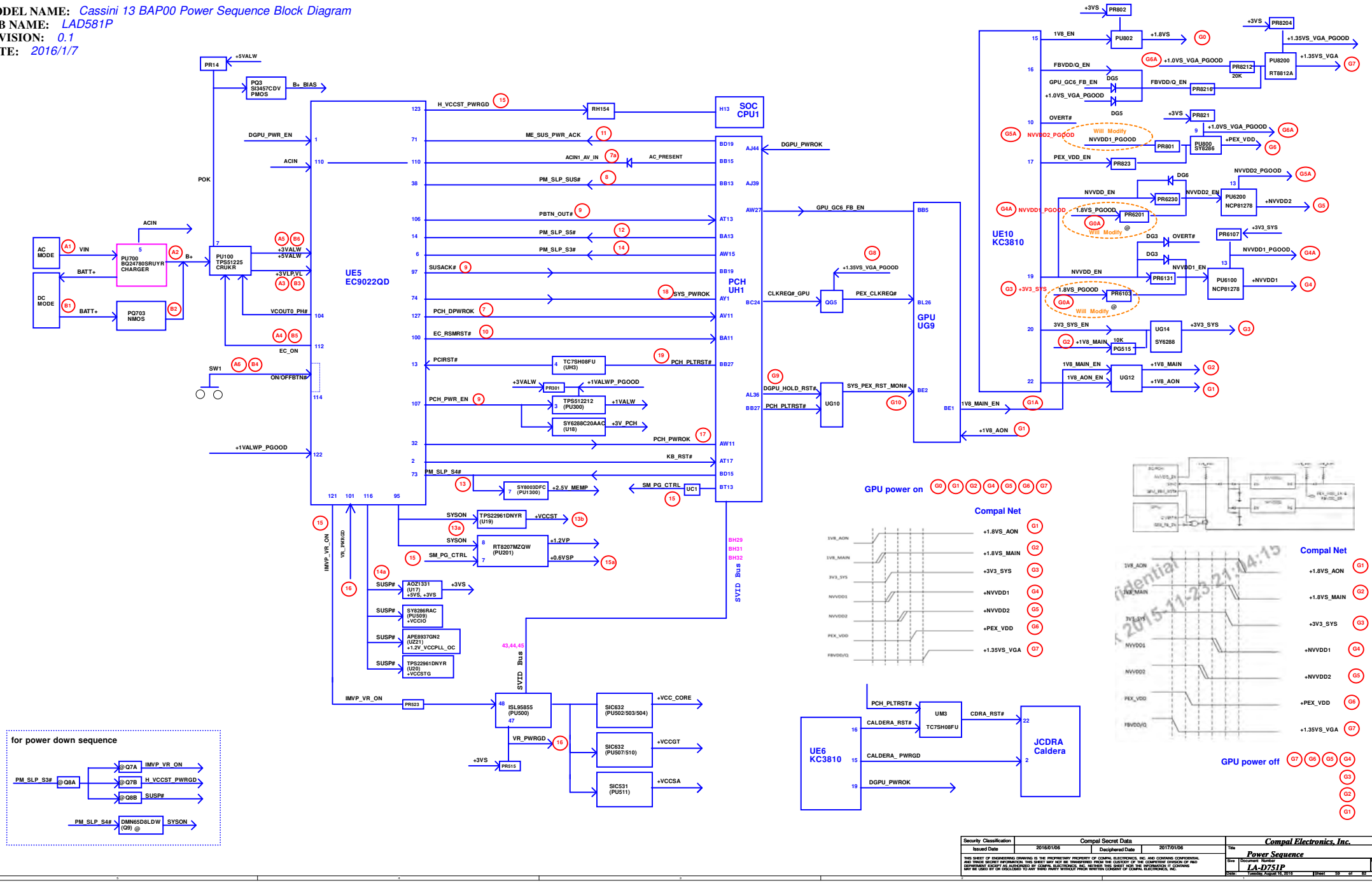
Date: Tuesday, August 16, 2016 | Sheet 57 of 82


Change DT1 and add DT15 follow E-team's design for DELL dat.04/07
Delete RT96 for layout @12/31
Close to UT4
60mil 3A
60mil 3A
Master:0 ohm
Slave1:93.1K ohm
TPS65982_BGA96
JUSBC1
CONN@ JAE_DX07S024JJ5_24P-T
TOP
Bottom
MCM1012B900F06BP 4P
TVWDF1004AD0_DFN8
Security Classification
Compal Secret Data
Issued Date
2016/01/06
Deciphered Date
2017/01/06
Compal Electronics, Inc.
PD+USB3.1 type C
LA-D751P
Rev 1.0
Tuesday, August 16, 2016
Sheet 58 of 82

MODEL NAME: *Cassini 13 BAP00 Power Sequence Block Diagram*
PCB NAME: *LAD581P*
REVISION: *0.1*
DATE: *2016/1/7*



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/01/06	Deciphered Date	2017/01/06
Title	Power Sequence		
Size	Document Number		Rev 1.0
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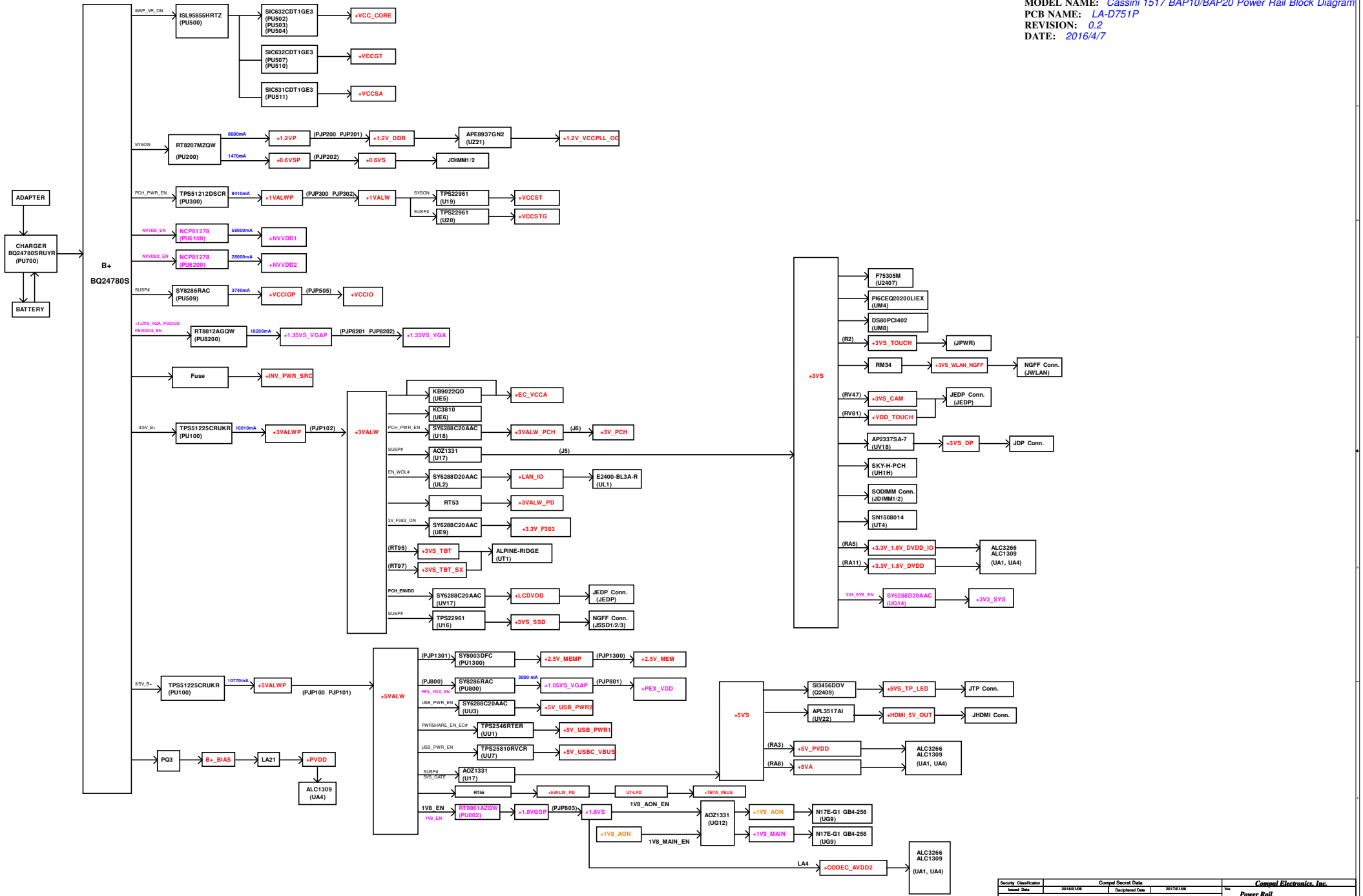
MODEL NAME: *Cassini 1517 BAP10/BAP20 Power Rail Block Diagram*
PCB NAME: *LA-D751P*
REVISION: *0.2*
DATE: *2016/4/7*



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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title: Power Rail
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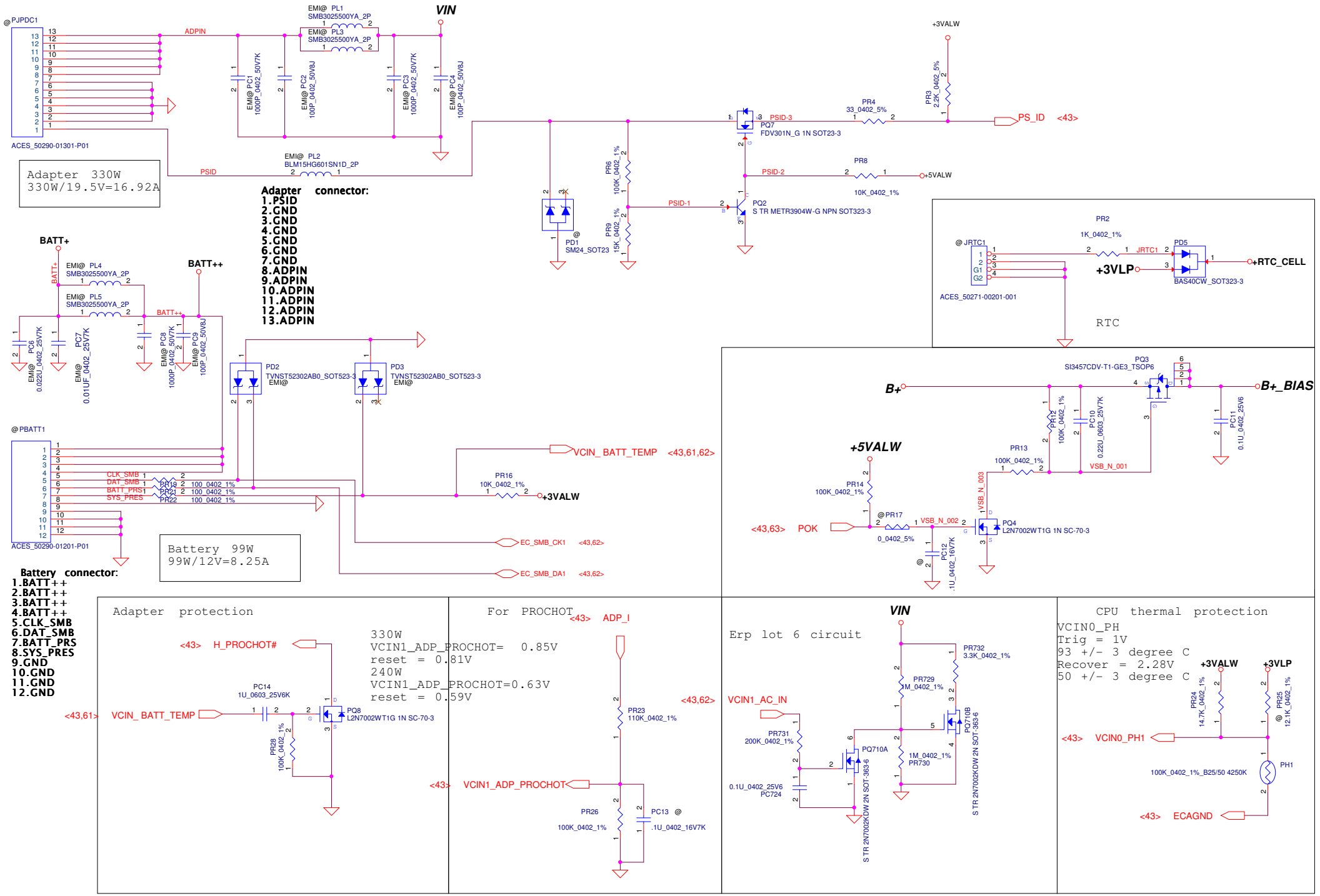
			Date: Tuesday, August 16, 2016	Sheet: 60 of 60



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **PWR-DCIN / BATT CONN / OTP**

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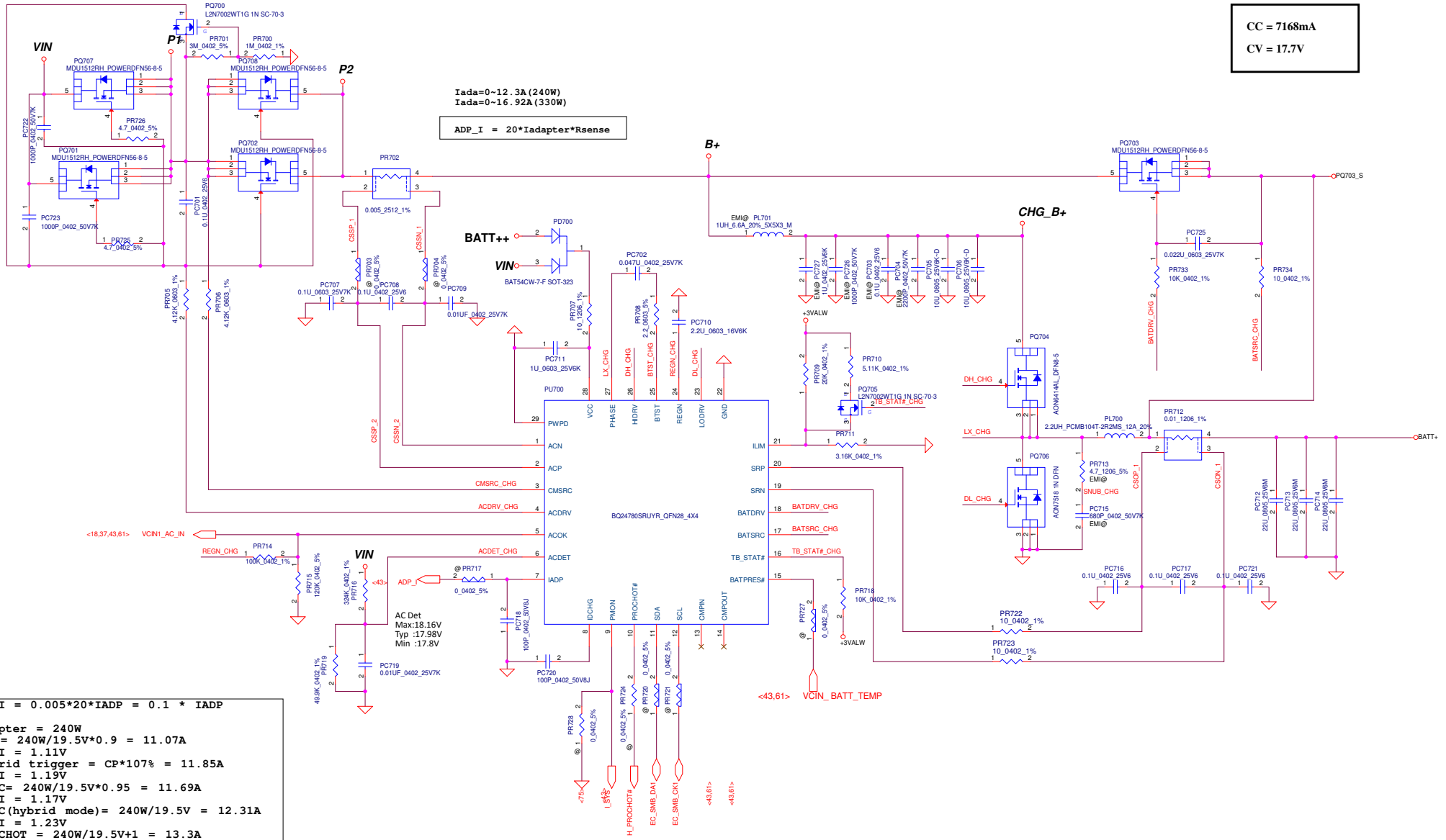

ADPI = 0.005*20*IADP = 0.1 * IADP

Adapter = 240W
CP = 240W/19.5V*0.9 = 11.07A
ADPI = 1.11V
Hybrid trigger = CP*107% = 11.85A
ADPI = 1.19V
IPCC= 240W/19.5V*0.95 = 11.69A
ADPI = 1.17V
IPCC(hybrid mode)= 240W/19.5V = 12.31A
ADPI = 1.23V
PROCHOT = 240W/19.5V+1 = 13.3A
ADPI = 1.33V

Adapter = 330W
CP = 330W/19.5V*0.9 =15.23 A
APDI = 1.52V
Hybrid trigger = CP*107% = 16.3A
ADPI = 1.63V
IPCC = 330W/19.5V*(1*0.95) = 16.08A
ADPI = 1.61V
IPCC(hybrid mode)= 330W/19.5V = 16.92A
ADPI = 1.69V
PROCHOT = 330W/19.5V+1 = 17.92A
ADPI = 1.79V

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PWR_CHARGER

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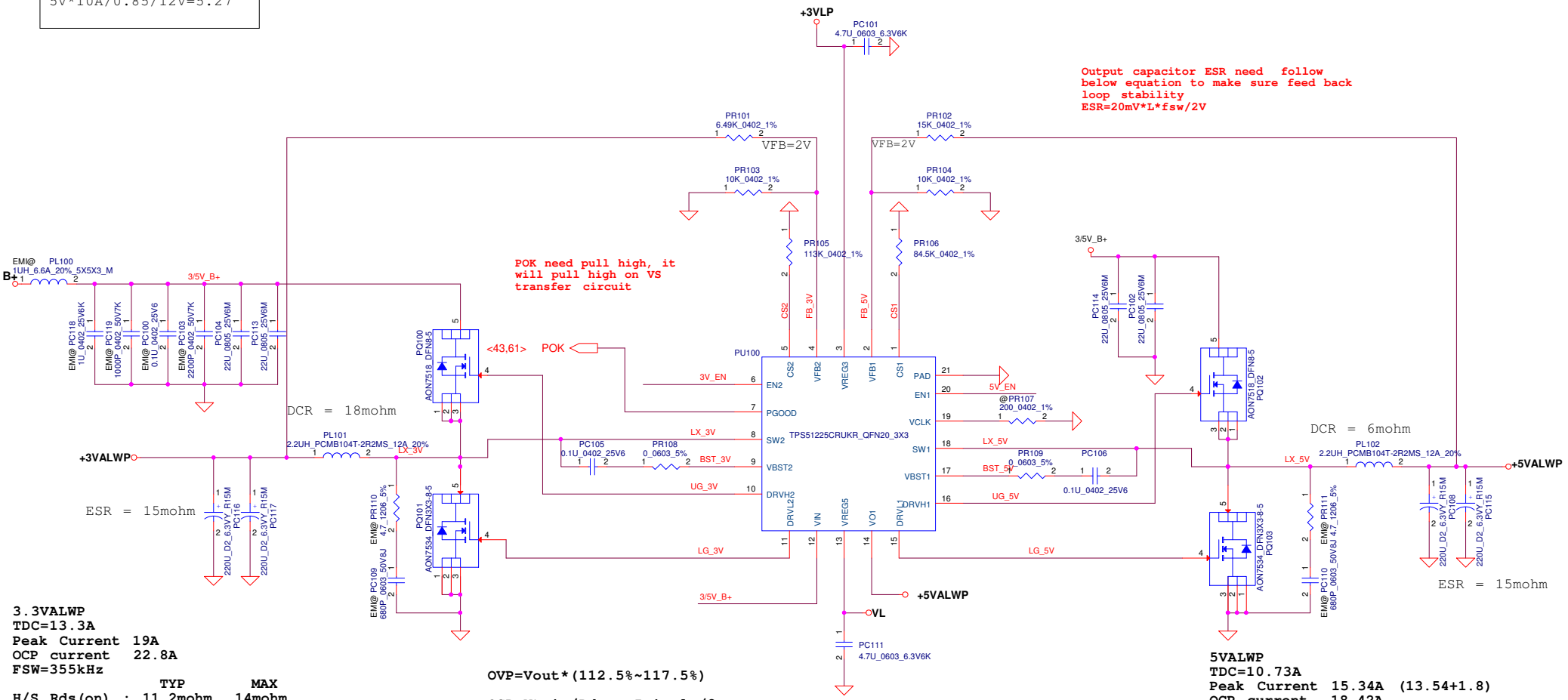
Input Current: 7.5A
3.3V*10A/0.85/12V=2.23
5V*10A/0.85/12V=5.27

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

POK need pull high, it will pull high on VS transfer circuit



3.3VALWP
TDC=13.3A
Peak Current 19A
OCP current 22.8A
FSW=355kHz

	TYP	MAX
H/S Rds(on)	11.2mohm	14mohm
L/S Rds(on)	6.7mohm	8.5mohm

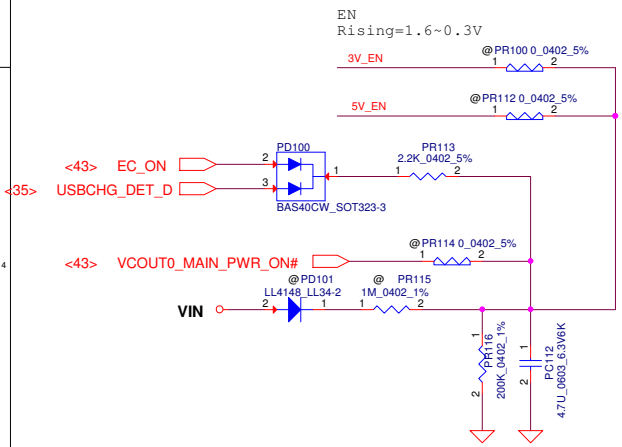
OVP=Vout*(112.5%~117.5%)

OCP=Vtrip/Rdson+Iripple/2
Vtrip=Ics(min)*Rcs/8+1mV
Vcs=Ics*vcs should be in the range of 0.2~2V

Vout=VFB*(1+Rtop/Rbot)
VFB=2V

5VALWP
TDC=10.73A
Peak Current 15.34A (13.54+1.8)
OCP current 18.42A
FSW=300kHz

	TYP	MAX
H/S Rds(on)	11.2mohm	14mohm
L/S Rds(on)	6.7mohm	8.5mohm



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Compal Electronics, Inc.

Title: PWR_3.3VALWP/5VALWP

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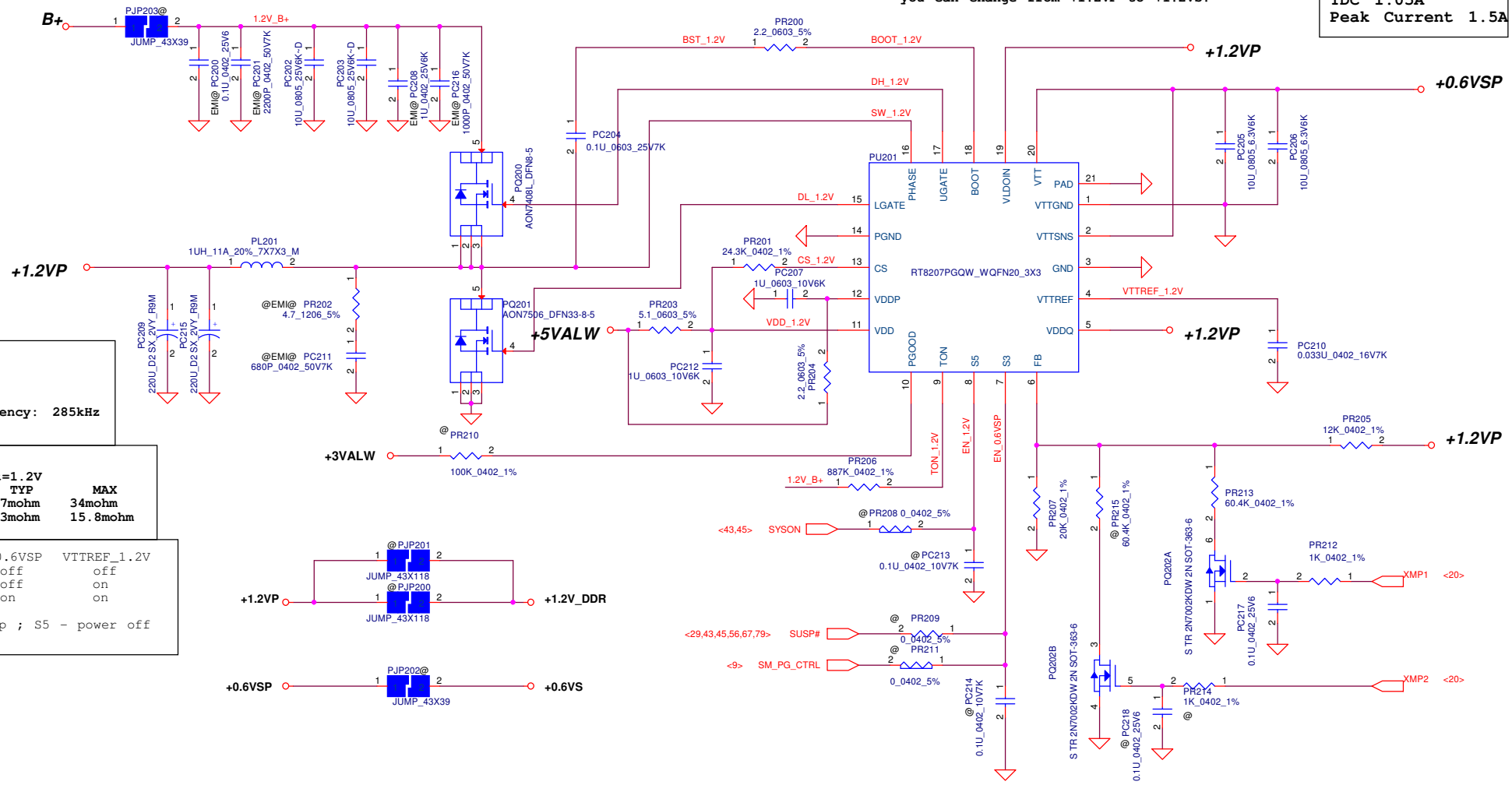
Input Current: 1A
1.2V*8.88A/0.85/12V=1

Pin19 need pull separate from +1.2VP.
If you have +1.2V and +0.6V sequence question,
you can change from +1.2VP to +1.2VS.

+0.6VSP
TDC 1.05A
Peak Current 1.5A



+1.2VP
TDC=9A
Ipeak=12.86A
OCP=15.43A
Switching Frequency: 285kHz

OVP: 110%~120%
VFB=0.75V, Vout=1.2V

	TYP	MAX
H/S Rds(on) :	27mohm	34mohm
L/S Rds(on) :	13mohm	15.8mohm

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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Title: PWR_1.2VP/0.6VSP

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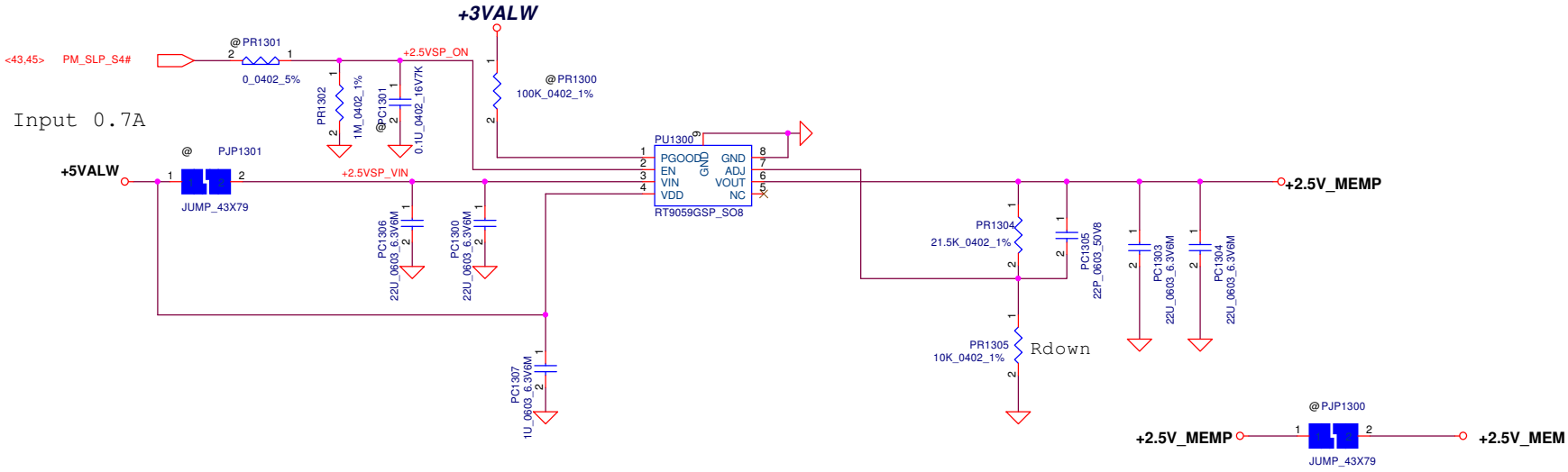

+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A

Vout=0.8V* (1+Rup/Rdown)

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Title: PWR_+2.5V_MEM

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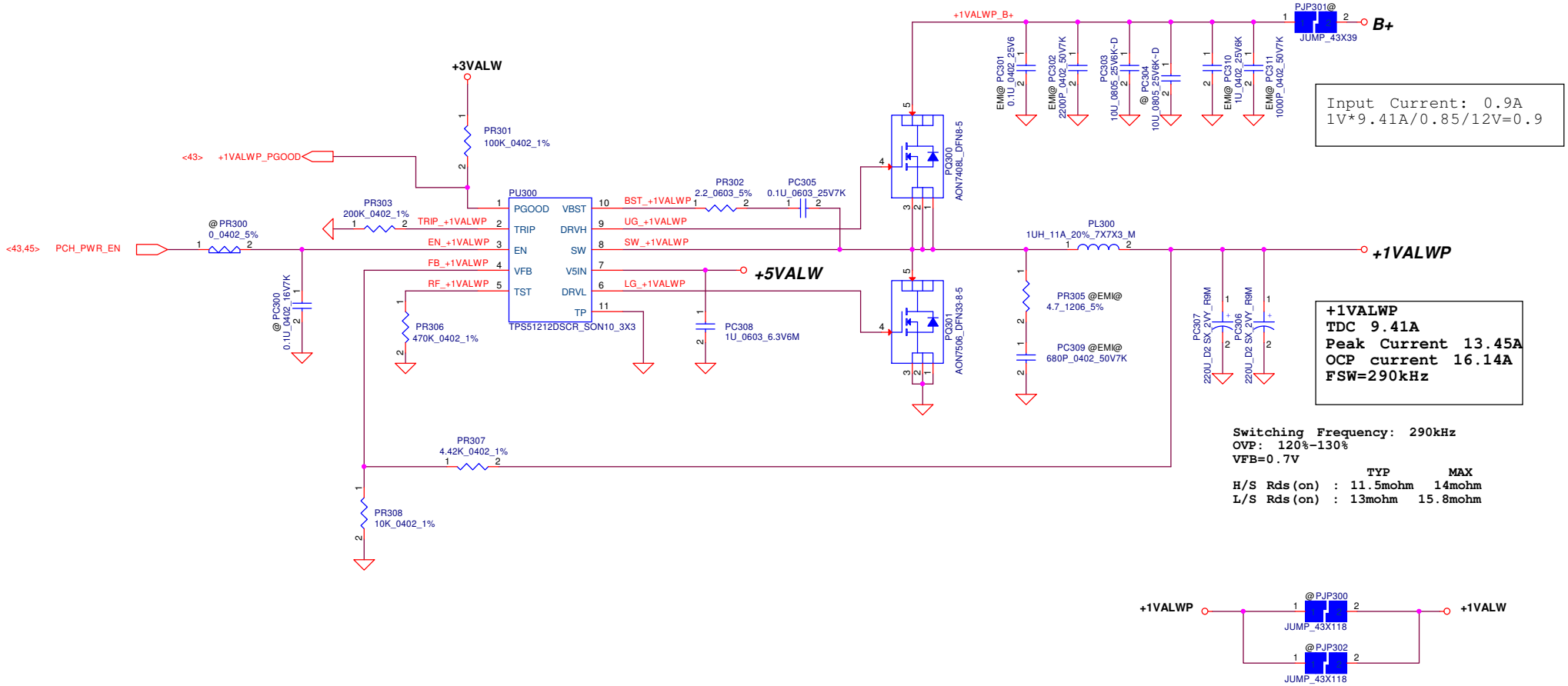

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Title: **PWR_+1VALWP**

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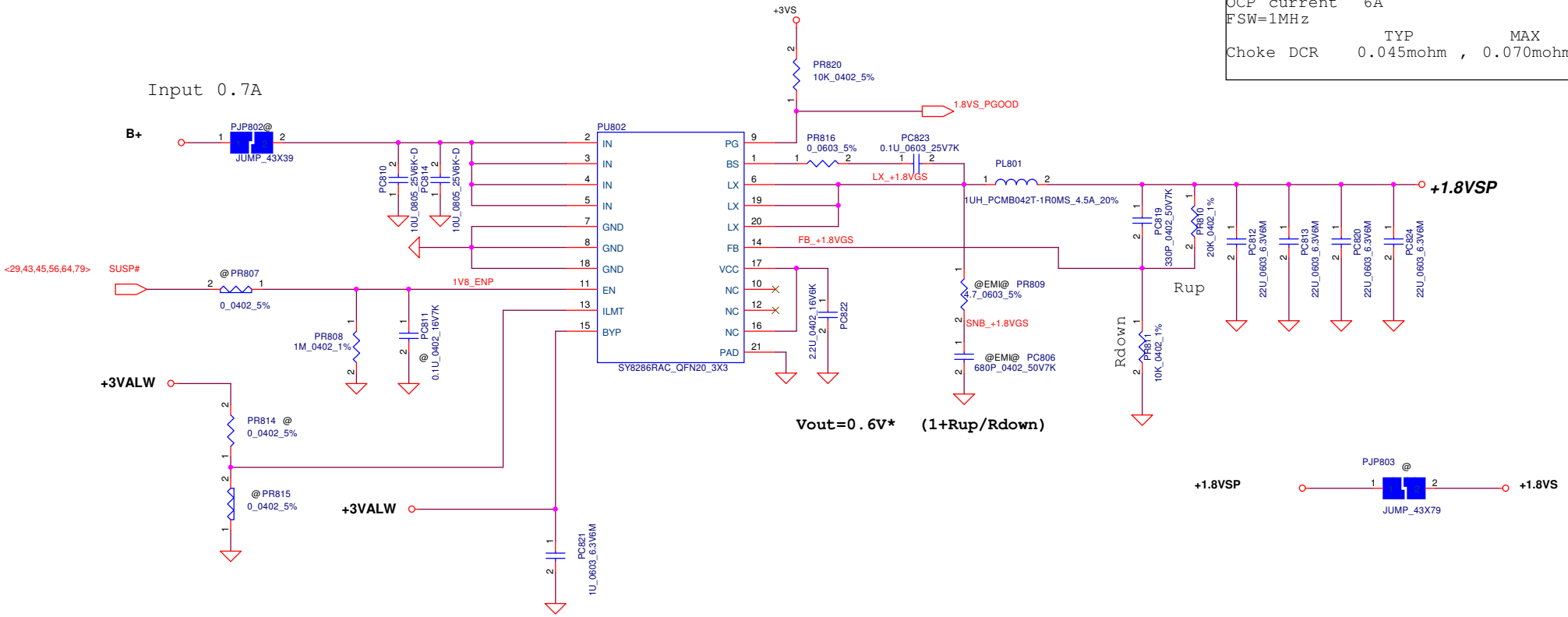

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Title: **PWR +1.8VSP**

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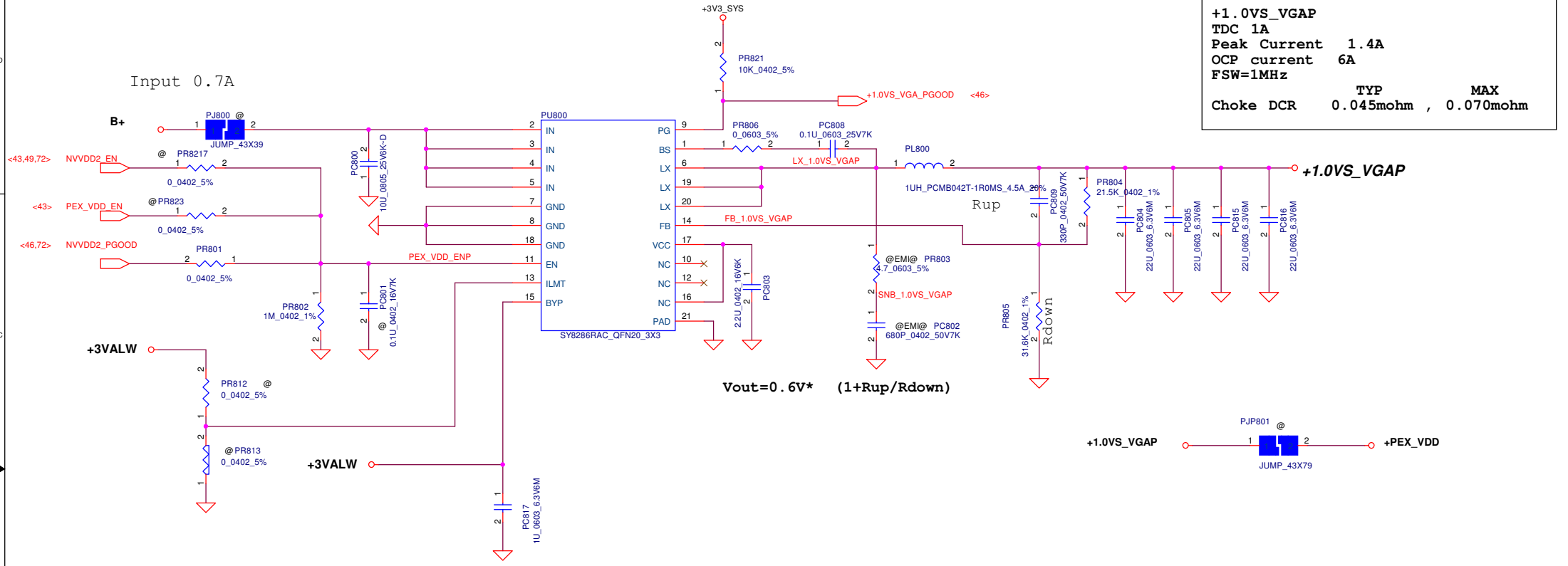

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Compal Electronics, Inc.

Title: PWR_+1.0VS_VGA

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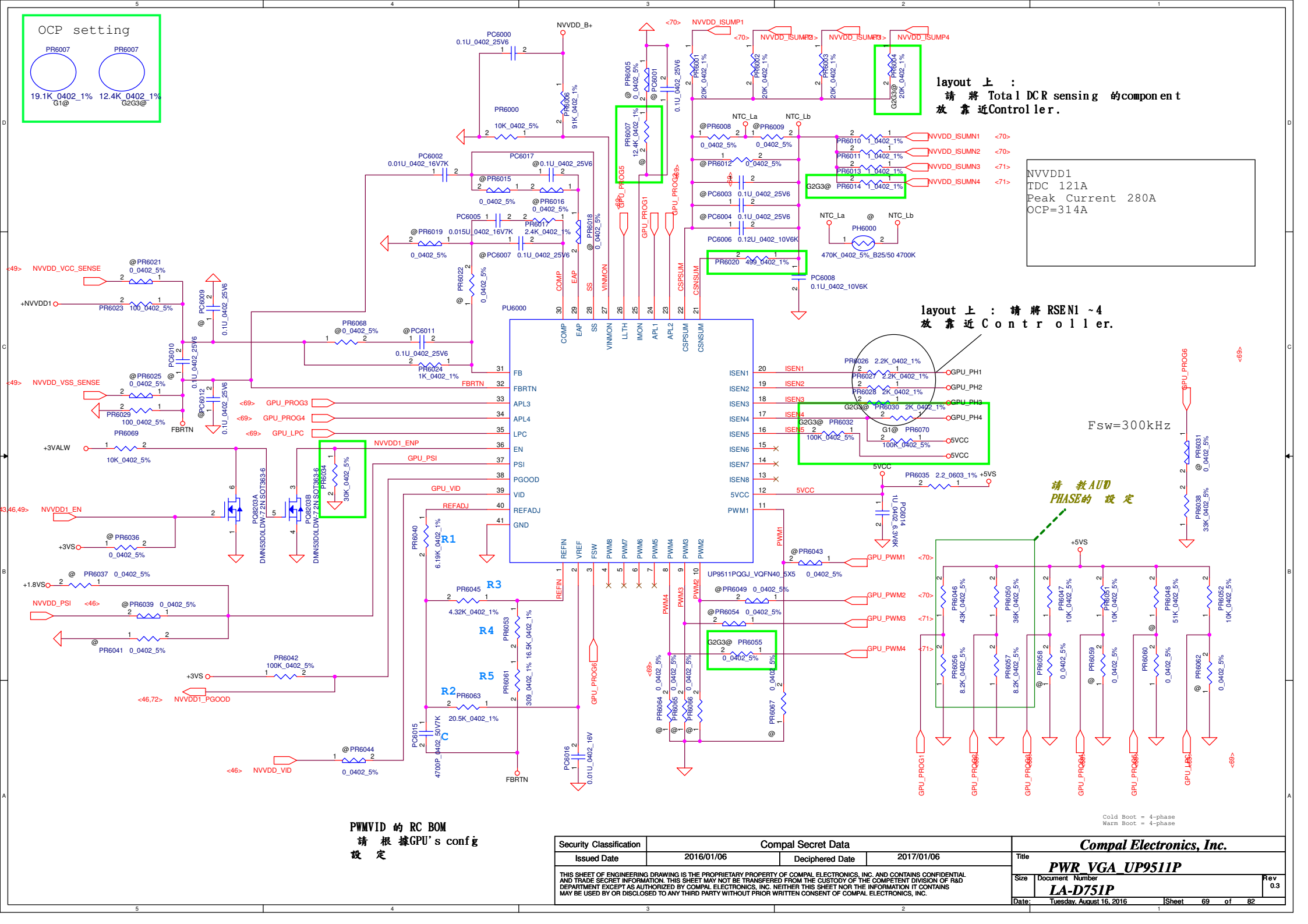
OCP setting
PR6007
PR6007
19.1K_0402_1%
G1@
12.4K_0402_1%
G2G3@
layout 上 : 請 將 Total DCR sensing 的component 放 靠 近Controller.
NVVDD1
TDC 121A
Peak Current 280A
OCP=314A
layout 上 : 請 將 RSEN1 ~4 放 靠 近 Controller.
Fsw=300kHz
請 教AUD PHASE的 設 定
PU6000
UP9511PQGJ_VQFN40_5X5
NVVDD_B+
NVVDD_VCC_SENSE
NVVDD_VSS_SENSE
+NVVDD1
+3VALW
NVVDD1_EN
NVVDD_PSI
NVVDD_VID
NVVDD1_PGOOD
GPU_PSI
GPU_VID
GPU_LPC
NVVDD1_ENP
GPU_PWM1
GPU_PWM2
GPU_PWM3
GPU_PWM4
GPU_PH1
GPU_PH2
GPU_PH3
GPU_PH4
FBRTN
5VCC
+5VS
+3VS
+1.8VS
R1
R2
R3
R4
R5
C
PWMVID 的 RC BOM 請 根 據GPU's config 設 定
Cold Boot = 4-phase
Warm Boot = 4-phase
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2016/01/06
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2017/01/06
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Title
PWR_VGA_UP9511P
Size
Document Number
LA-D751P
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0.3
Date: Tuesday, August 16, 2016
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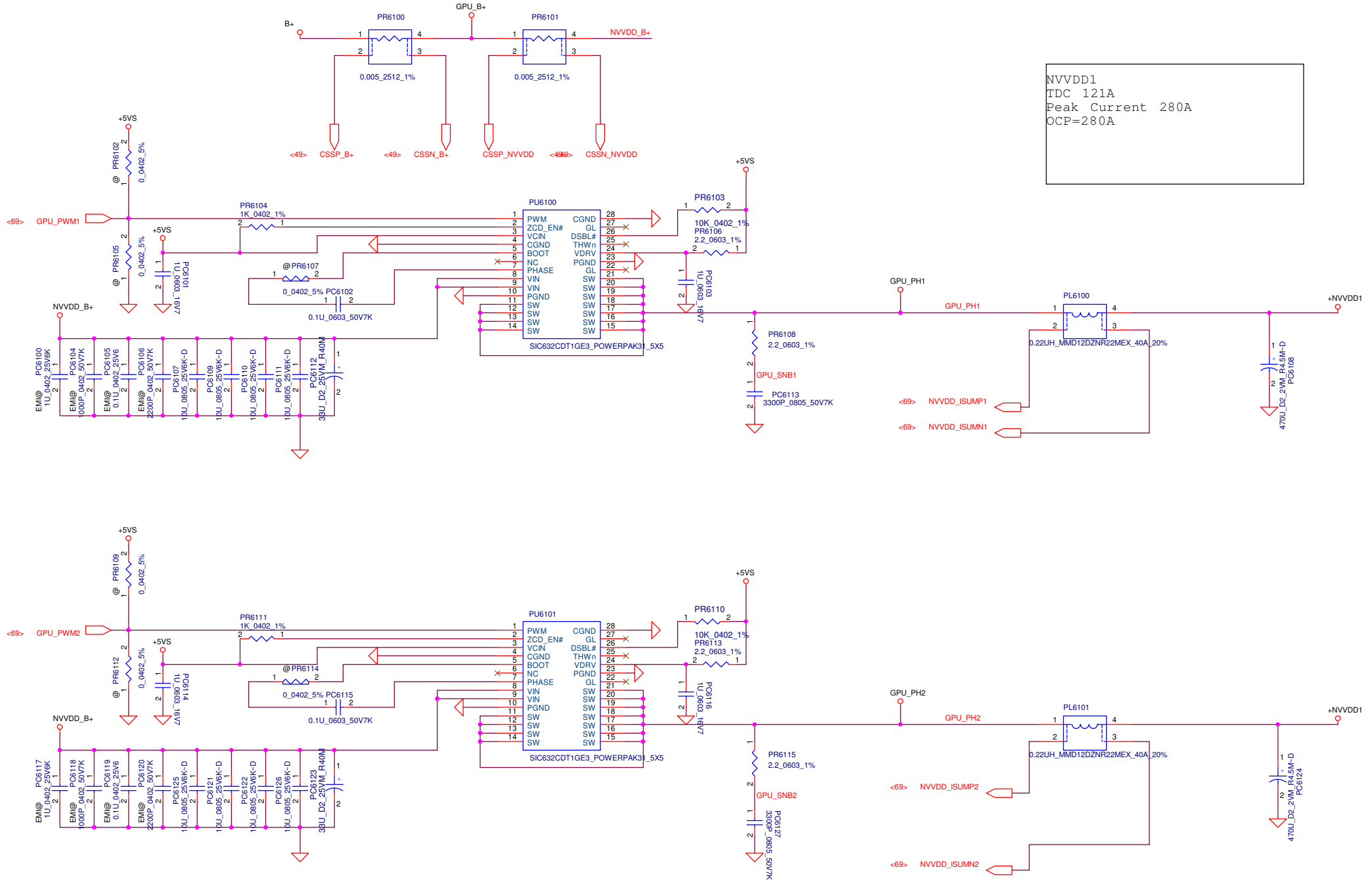

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Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size	Document Number	Rev
	LA-D751P	0.3

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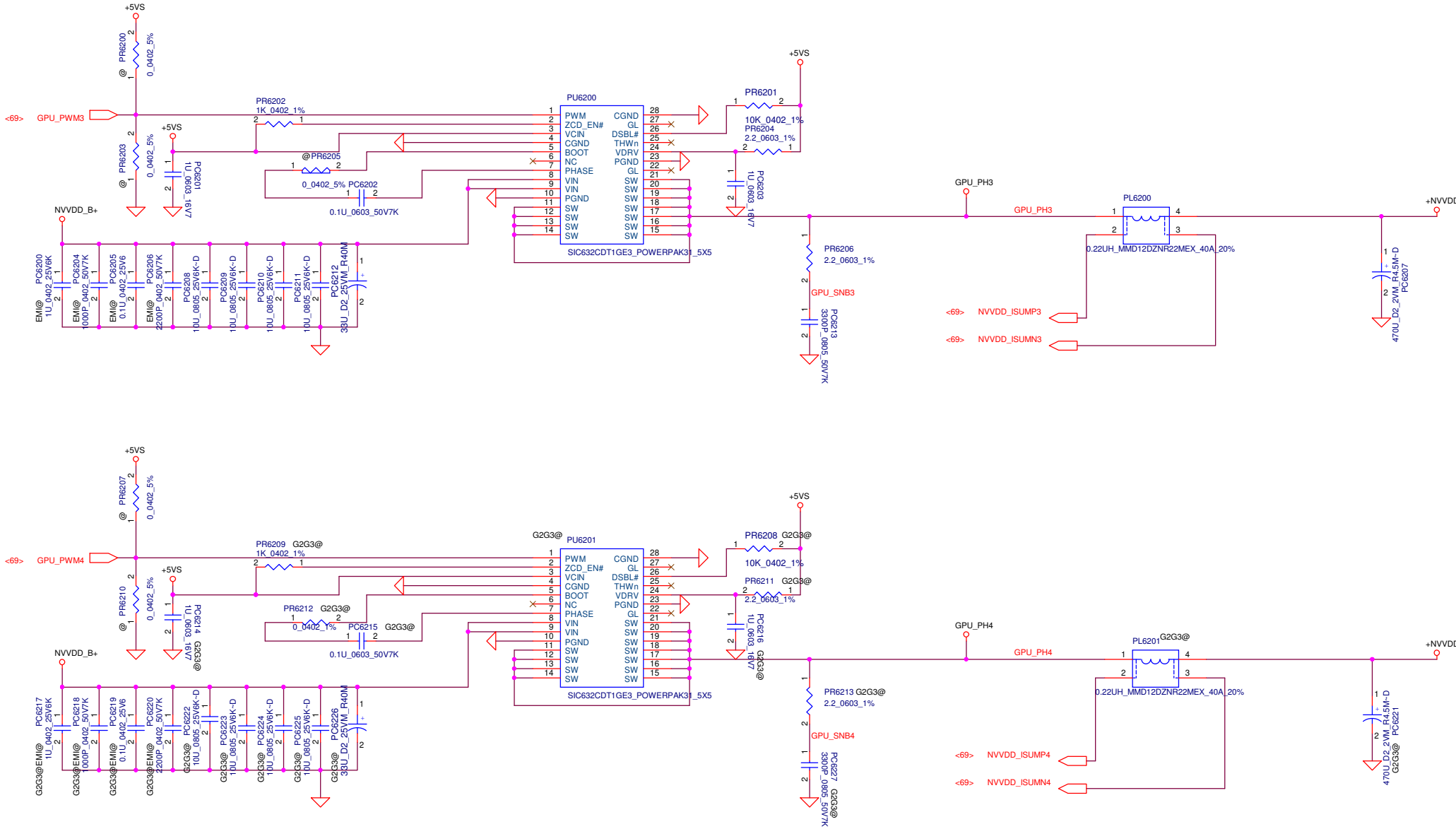

Security Classification	Compal Secret Data		
Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **PWR_+NVVDD1**

Size	Document Number	Rev
	LA-D751P	0.3

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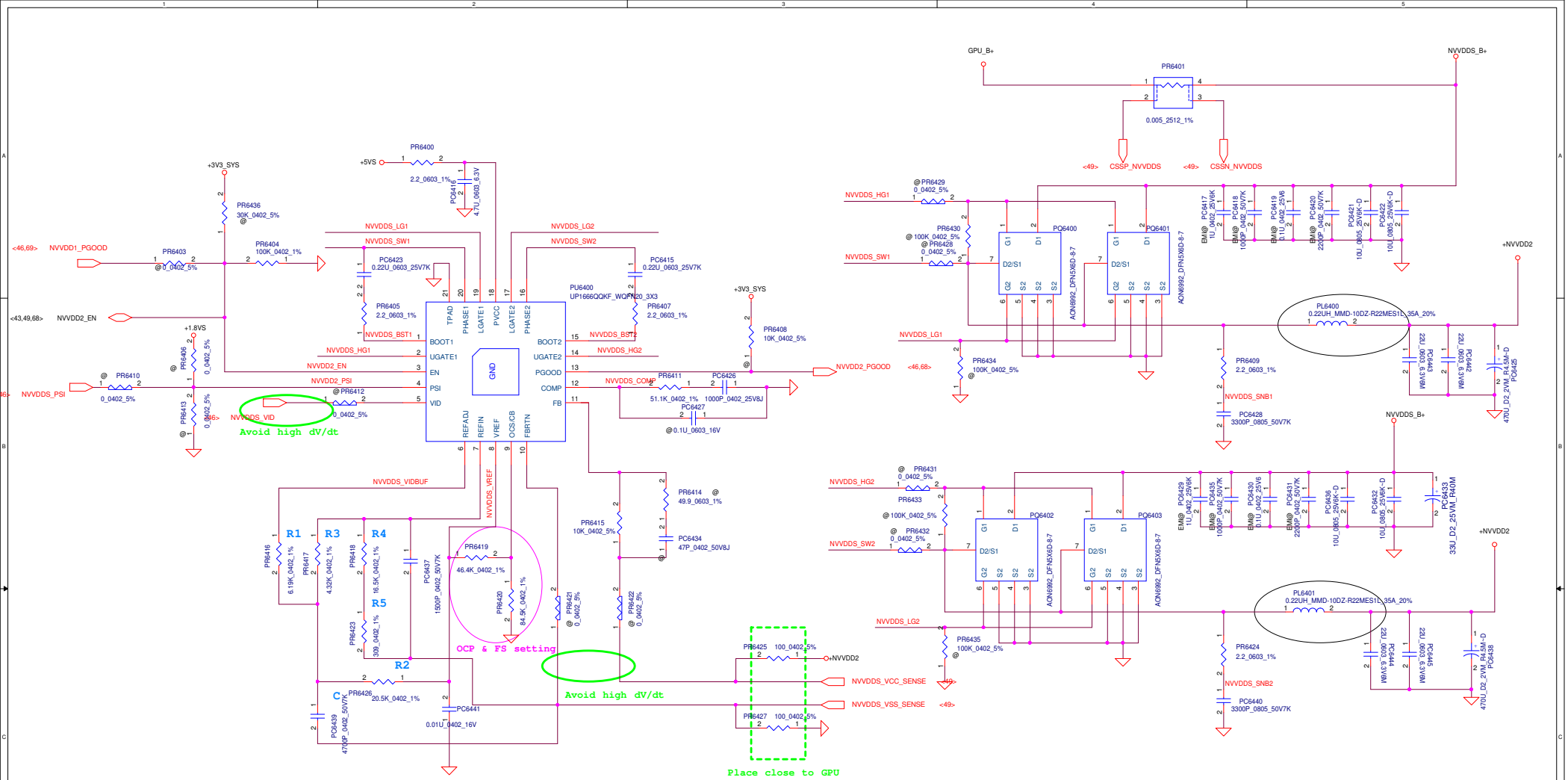

NVVDD2
TDC 37A
Peak Current 84A
OCP=108A

	TYP	MAX
H/S Rds(on):	6.7mohm	,8.5mohm
L/S Rds(on):	2mohm	,2.5mohm

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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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Compal Electronics, Inc.

Title: **PWR_+NVVDD2**

Size	Document Number	Rev
	LA-D751P	0.3

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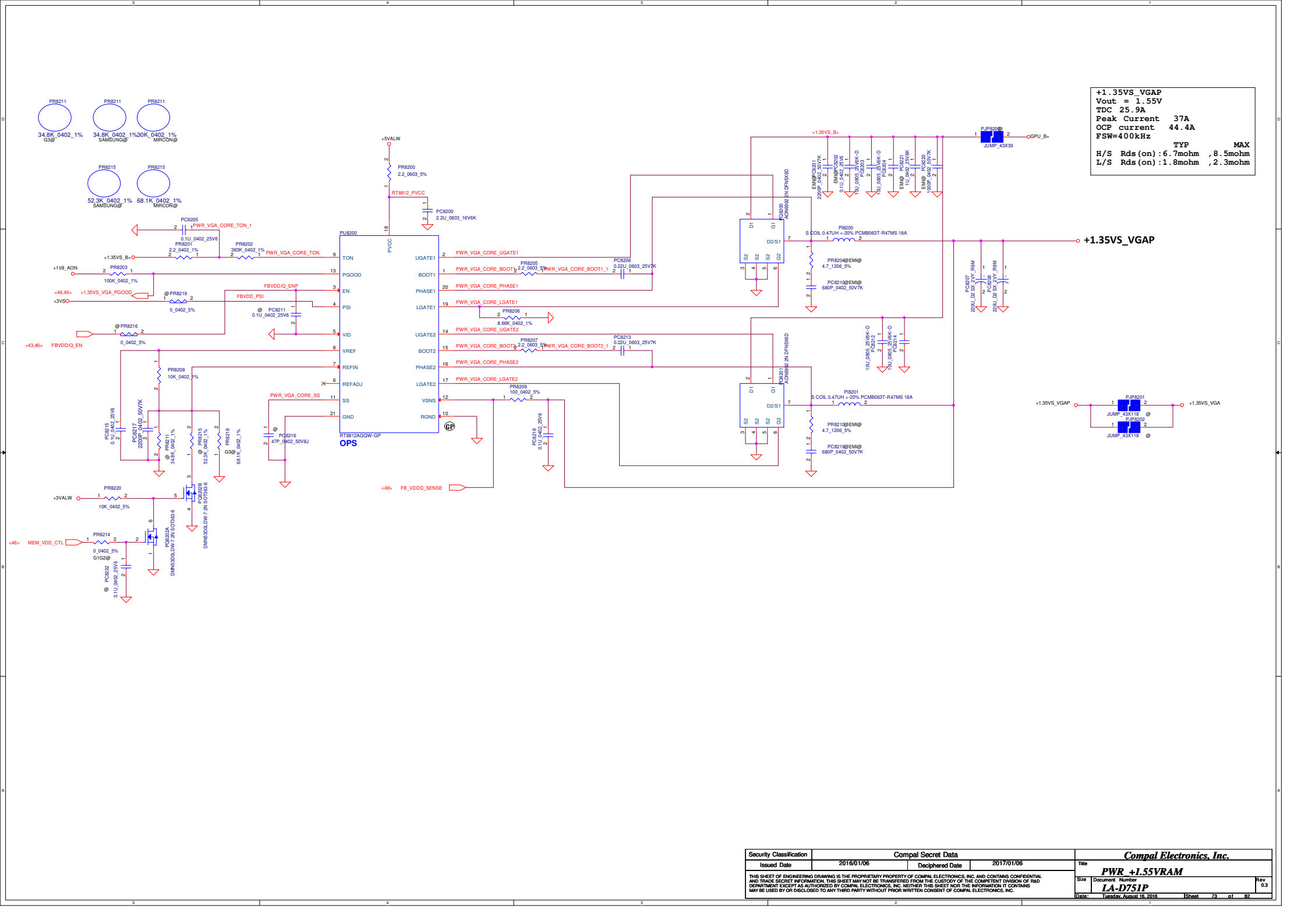

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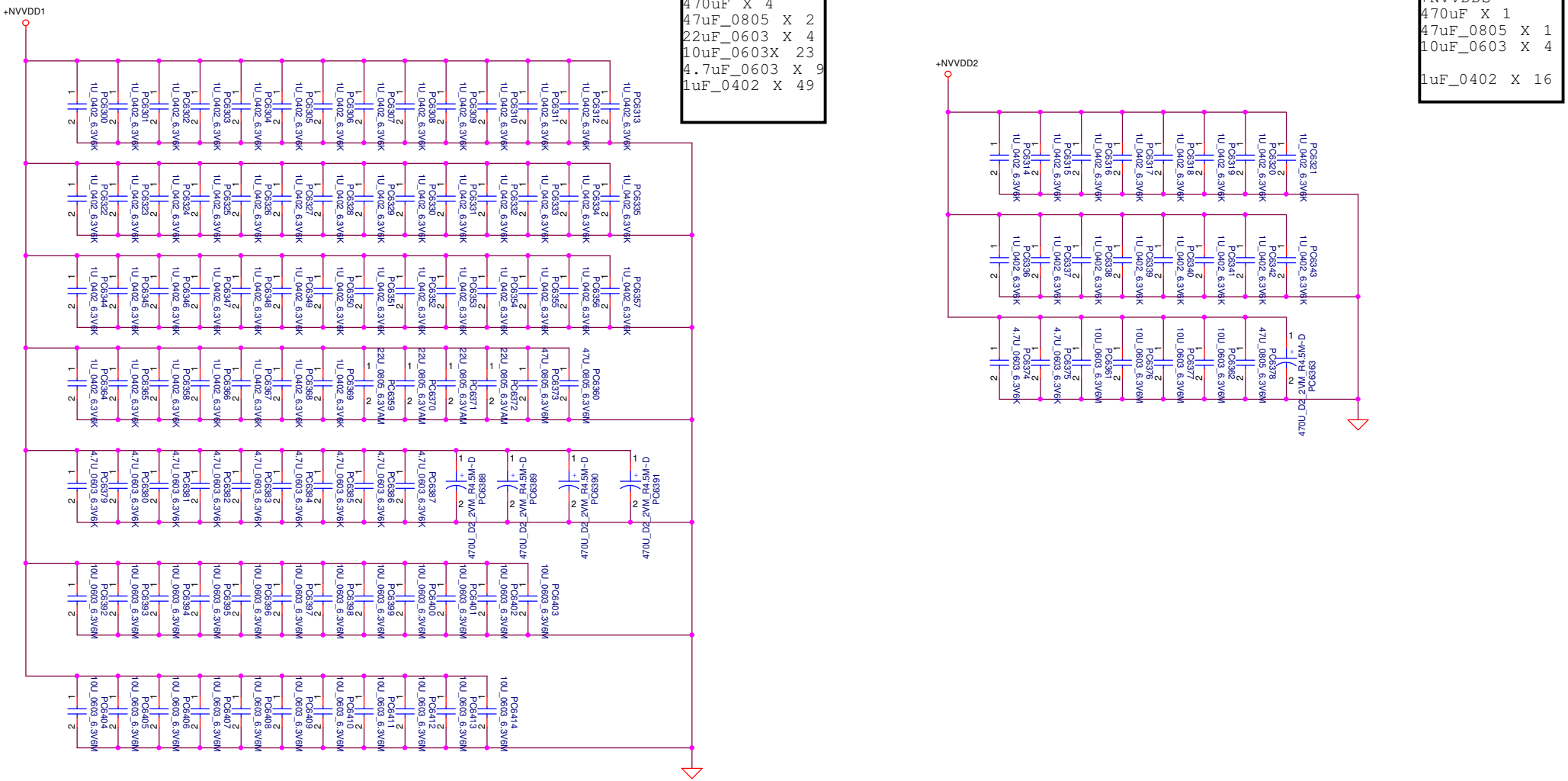
Compal Electronics, Inc.

Title: PWR +1.55VRAM

Size | Document Number: LA-D751P | Rev: 0.3

Date: Tuesday, August 16, 2016 | Sheet 73 of 82



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Issued Date	2016/01/06	Deciphered Date	2017/01/06

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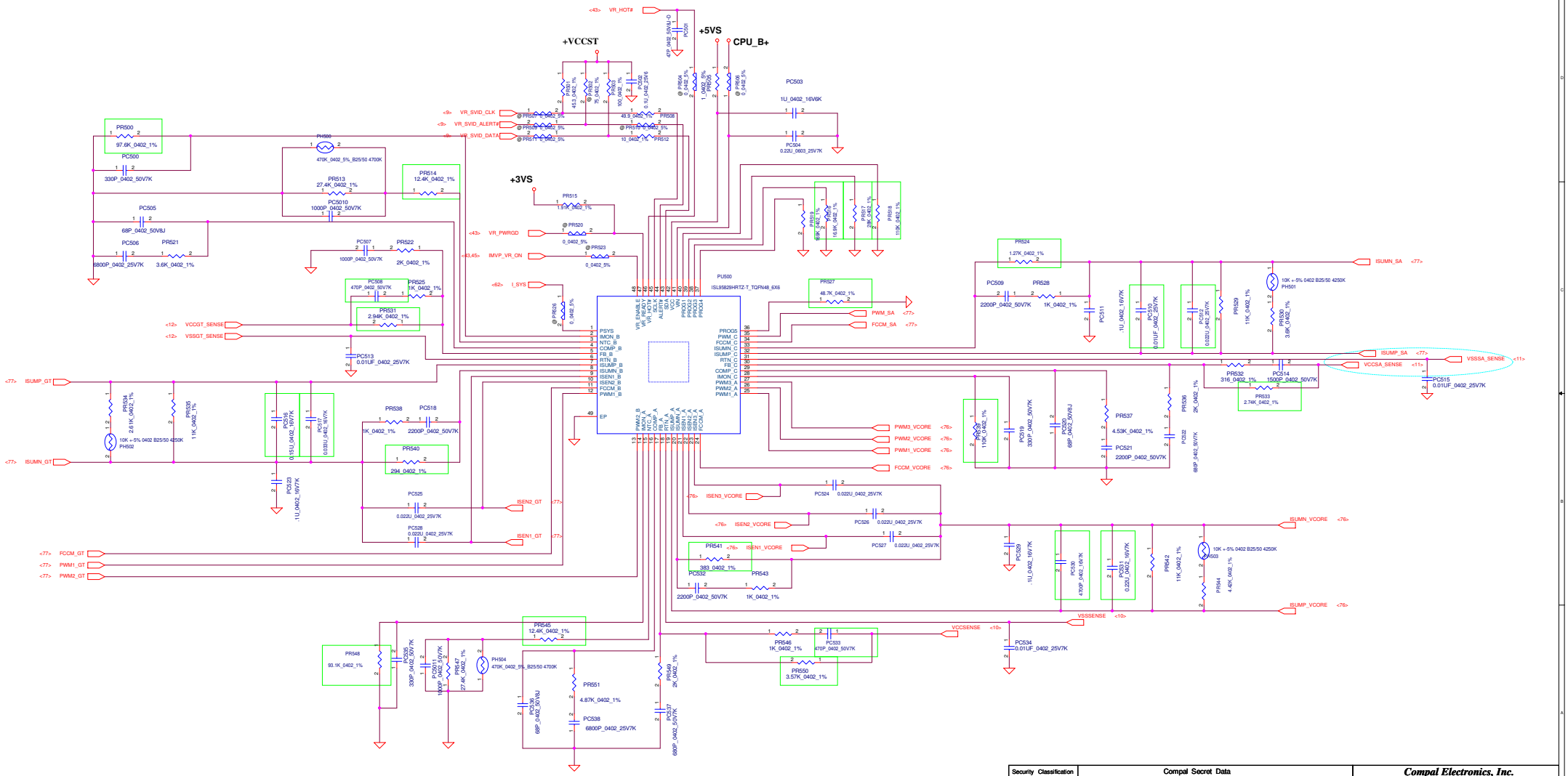
Compal Electronics, Inc.

Title: **PWR_VGA DECOUPLING**

Size	Document Number	Rev
	LA-D751P	0.3

Date: Tuesday, August 16, 2016 | Sheet 74 of 82



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Compal Electronics, Inc.

Title: **PWR_VCORE_ISL95855**

Size: | Document Number: **LA-D751P** | Rev: 0.3

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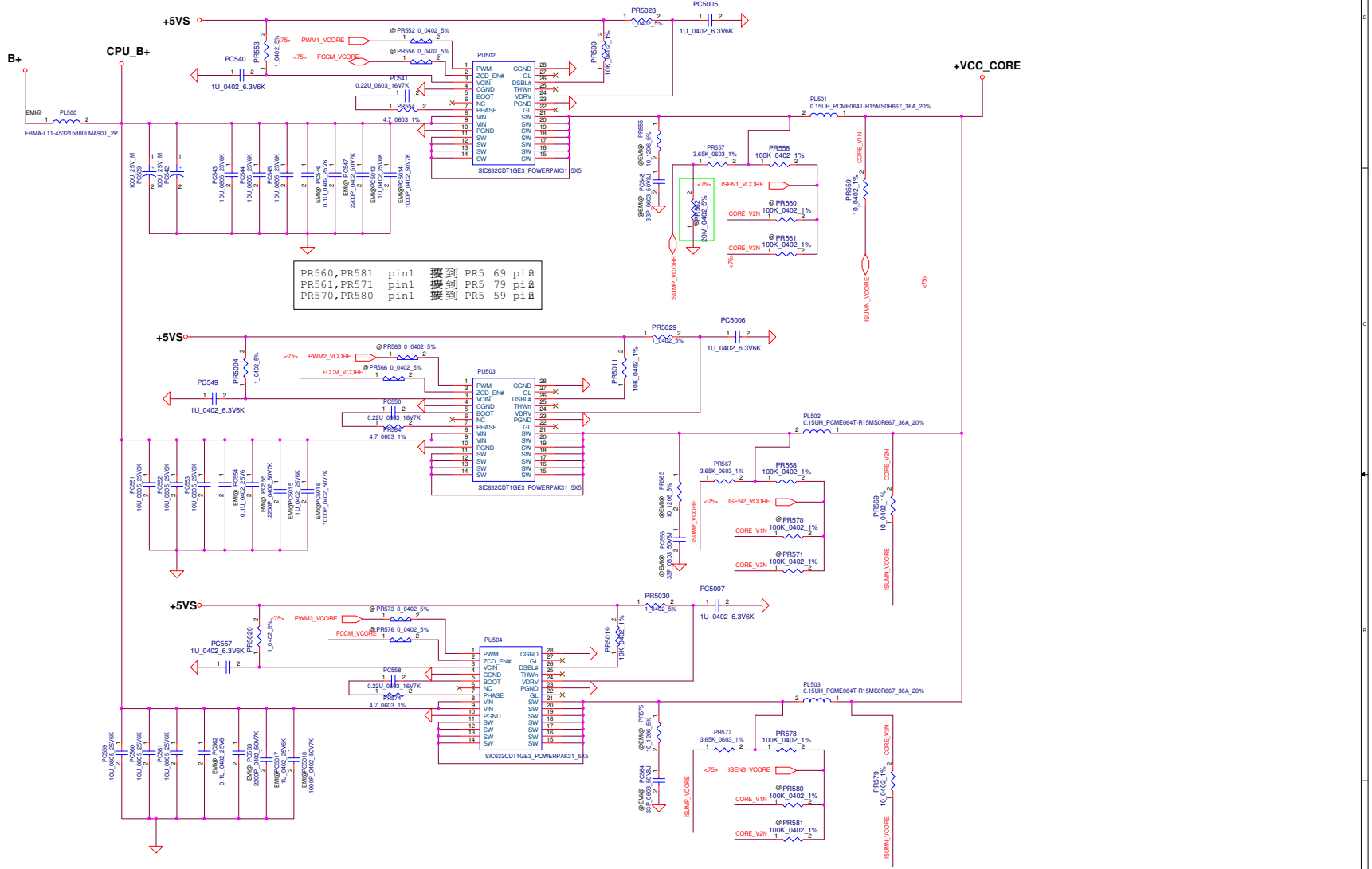
Input Current: 8.2A
1.5V*56A/0.85/12V=8.2

+VCC_CORE
TDC PL2 :56A
Peak Current 68A
OCP Current 81.6A
DCR 0.66mohm +/-7%
Load Line 1.8mV/A



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Compal Electronics, Inc.

Title: PWR_VCORE_+VCC_CORE

Size	Document Number	Rev
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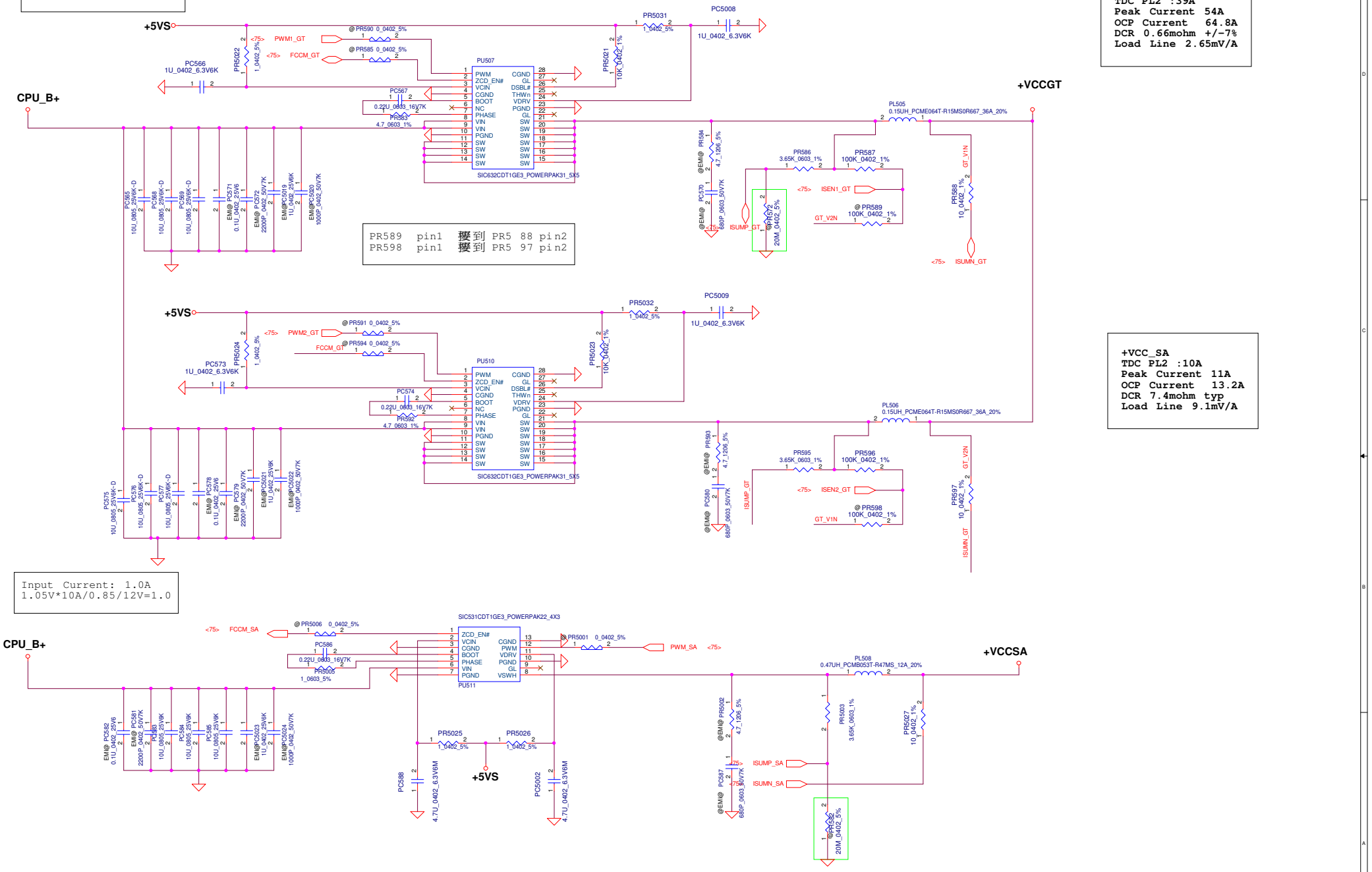
Input Current: 5.7A
1.5V*39A/0.85/12V=5.7

+VCC_GT
TDC PL2 :39A
Peak Current 54A
OCP Current 64.8A
DCR 0.66mohm +/-7%
Load Line 2.65mV/A

PR589 pin1 擺到 PR5 88 pin2
PR598 pin1 擺到 PR5 97 pin2

+VCC_SA
TDC PL2 :10A
Peak Current 11A
OCP Current 13.2A
DCR 7.4mohm typ
Load Line 9.1mV/A

Input Current: 1.0A
1.05V*10A/0.85/12V=1.0



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Compal Electronics, Inc.

Title: PWR_VCORE_+VCCGT,+VCCSA

Size	Document Number	Rev
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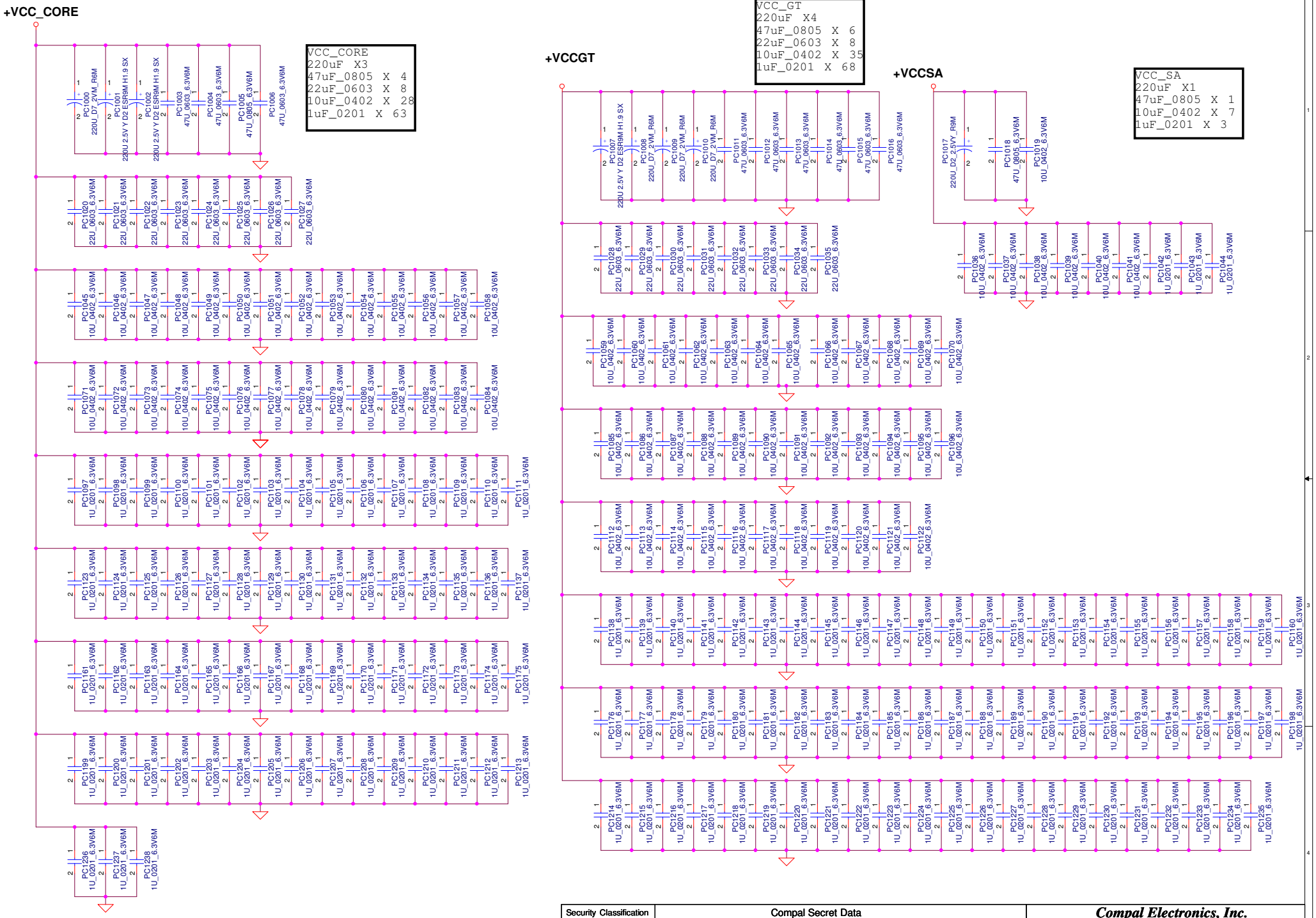

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Compal Electronics, Inc.

Title: **PWR-CPU DECOUPLING**

Size	Document Number	Rev
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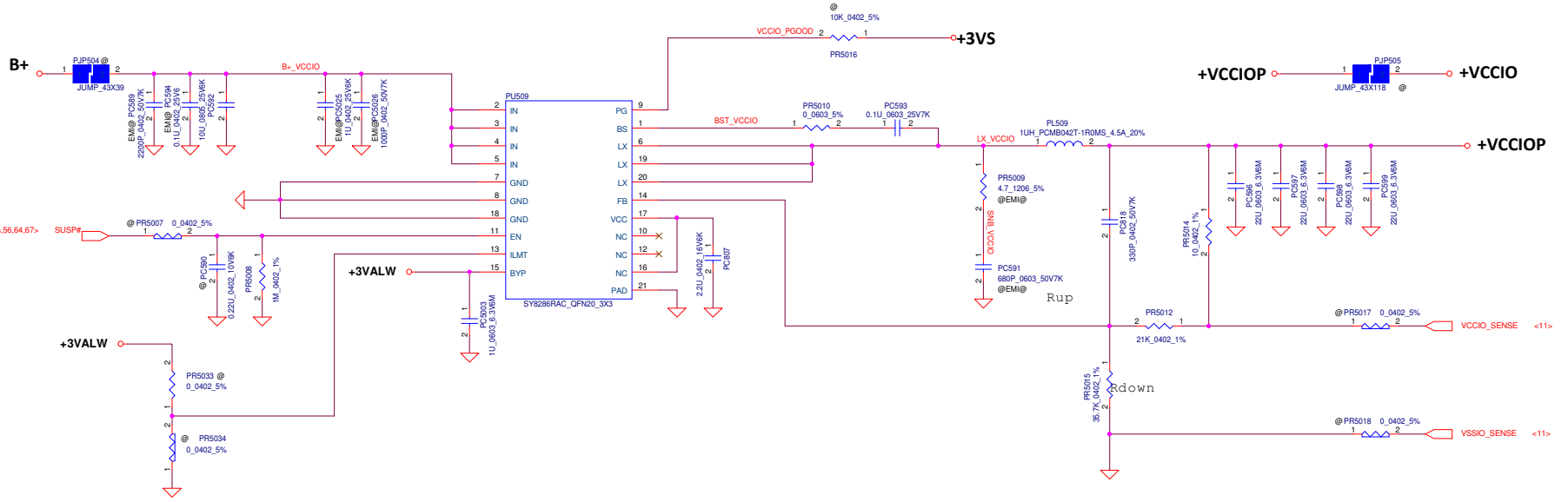

+VCCIOP (0.95V)
TDC 3.85 A
Peak Current 5.5 A
OCP Current 6 A Fix by IC

	TYP	MAX
Choke DCR	24.0mohm , 27.0mohm	

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Compal Electronics, Inc.

Title: **PWR_+VCCIO**

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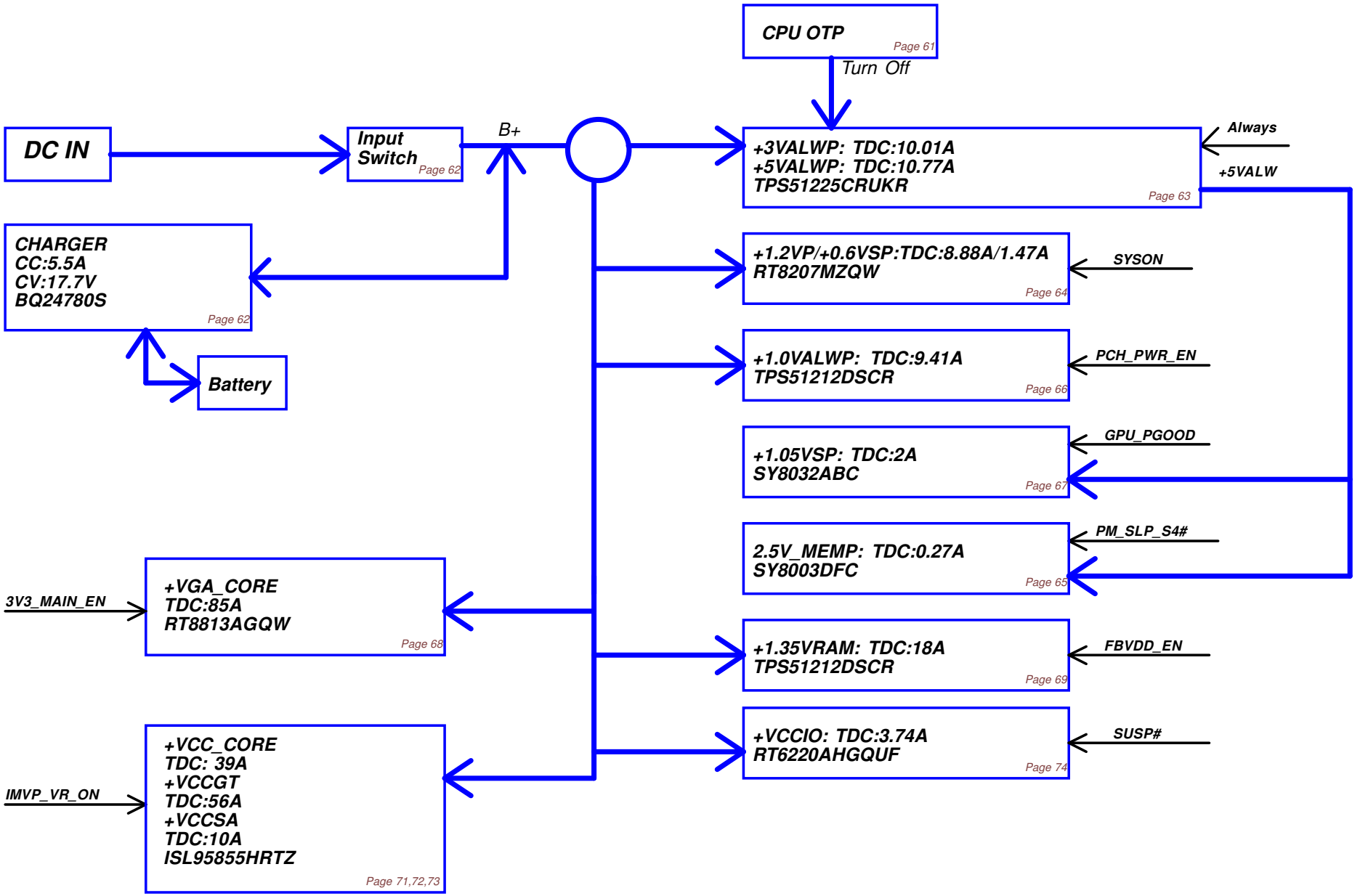
Power block



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Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

Size	Document Number	Rev
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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	69	VGA_UP9511P	2016/03/28	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6020 from 100 Ohm to 500 Ohm. 2. Change PR6007 from 5.1k Ohm to 13.3k Ohm	0.2
2	64	+1.2VP/+0.6VSP	2016/03/28	Compal_PWR	Add component for XMP	1. Change PR213 from 20k Ohm to 60.4k Ohm.	0.2
3	69	VGA_UP9511P	2016/03/30	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6069&PR6036 pin 1 from +3V3_SYS to +3VALW .	0.2
4	69	VGA_UP9511P	2016/04/01	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6033 connect to NVVDD_EN.	0.2
5	72	+NVVDD2	2016/04/01	Compal_PWR	For EE request to fine tune power sequence.	1. Change PR6402 connect to NVVDD_EN.	0.2
6	73	+1.35VS_VGAP	2016/04/11	Compal_PWR	For NV request.	1. Change +3VS to +1.8V_AON	0.2
7	64	+1.2VP/+0.6VSP	2016/04/11	Compal_PWR	Add component for XMP	1. Add PR212 to 1k Ohm. 2. Add PC217 to 0.1uF. 3. Add PQ202 MOS.	0.2
8	73	+1.35VS_VGAP	2016/04/11	Compal_PWR	For BOM control	1. Add PR8211 of 34.8k Ohm for SAMSUNG@ 2. Add PR8211 of 30k Ohm for MIRCON@ 3. Add PR8215 of 52.3k Ohm for SAMSUNG@ 4. Add PR8215 of 68.1k Ohm for MIRCON@ .	0.2
9	68	+1VS_VGAP	2016/04/11	Compal_PWR	For +1VS_VGAP OCP setting.	1. Change PL800 from 1UH_MAMK2520T1R0M_3.1A to 1UH_PCMB042T-1R0MS_4.5A.	0.2

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Compal Electronics, Inc.

Title: PWR_PIR1

Size | Document Number: LA-D751P | Rev: 0.3

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Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
10	75	VCORE_ISL95829	2016/05/18	Compal_PWR	For CPU_VCORE setting.	1. Change PC507 from 680pF to 1000pF. 2. Change PC517 from 0.047uF to 0.068uF. 3. Change PR548 from 95.3kohm to 105kohm.	0.3
11	62	CHARGER	2016/05/18	Compal_PWR	For CHARGER ILIM setting.	1. Change PR710 from 2kohm to 5.11kohm. 2. Change PR711 from 2.43kohm to 3.16kohm.	0.3
12	68	+1.0VS_VGAP	2016/05/18	Compal_PWR	Add component for +1.0VS_VGAP_EN	1. Add PR801 for 0ohm.	0.3
13	69	VGA_UP9511P	2016/05/18	Compal_PWR	For VGA_UP9511P_EN	1. Change PQ8203 from TR DMN66D0LDW-7 2N SOT363-6 to TR DMN53D0LDW-7 2N SOT363-6.	0.3
14	73	+1.55VRAM	2016/06/20	Compal_PWR	Add component for +1.55VRAM	1. Add PR8219 or 0ohm.	0.4
15	62	CHARGER	2016/06/20	Compal_PWR	For charger setting.	1. Add PQ701,PQ702,PQ707,PQ708,PQ703 of AON7506_DFN33-8-5 for X76@	0.4

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